COSMICi: High Energy Particle Detector

Group 5:

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Project Goal

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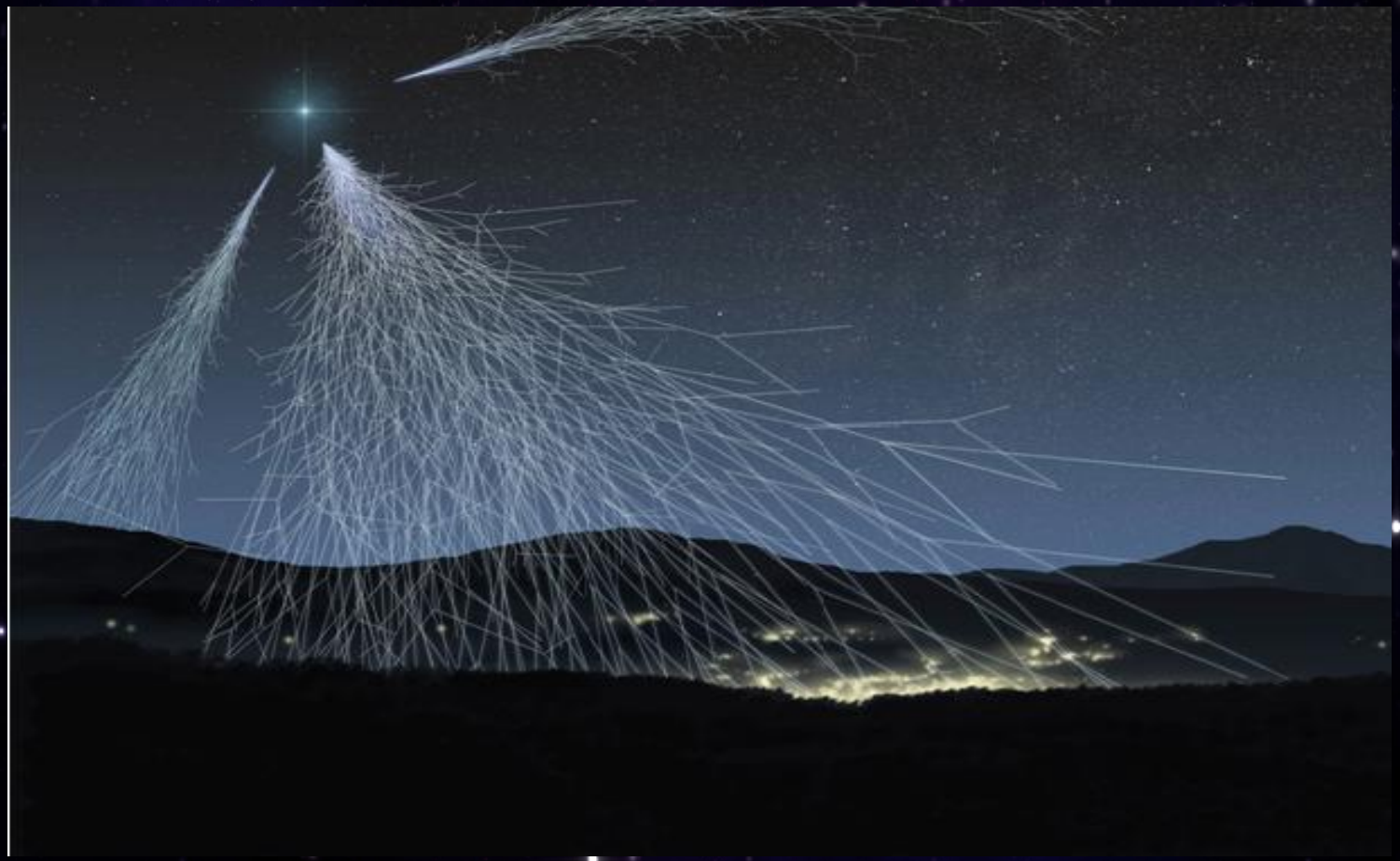
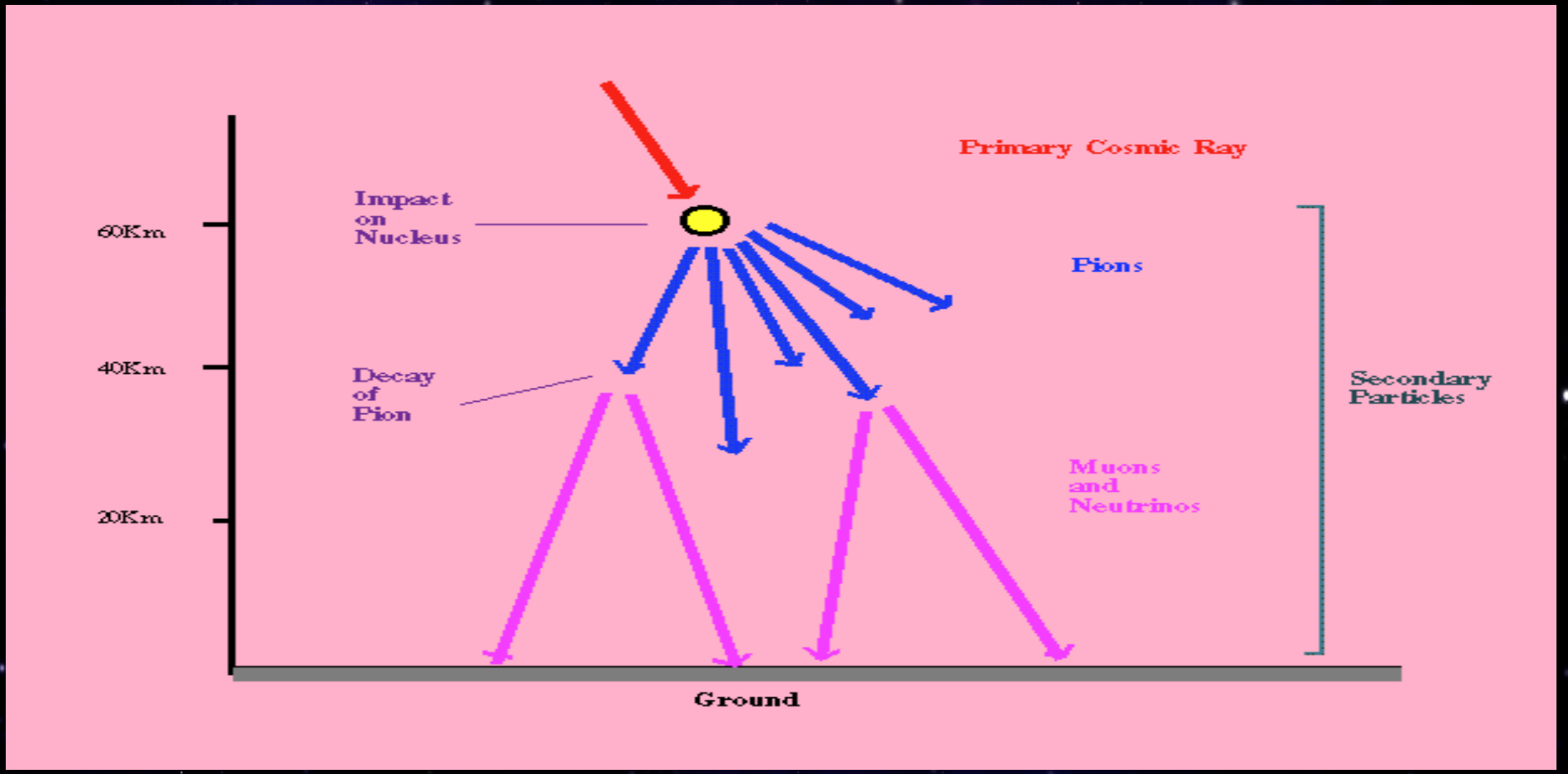
Project Goal

- Install and implement a network of Cosmic Ray detectors that will triangulate the origins of UHECR (Ultra High Energy Cosmic Rays) shower events



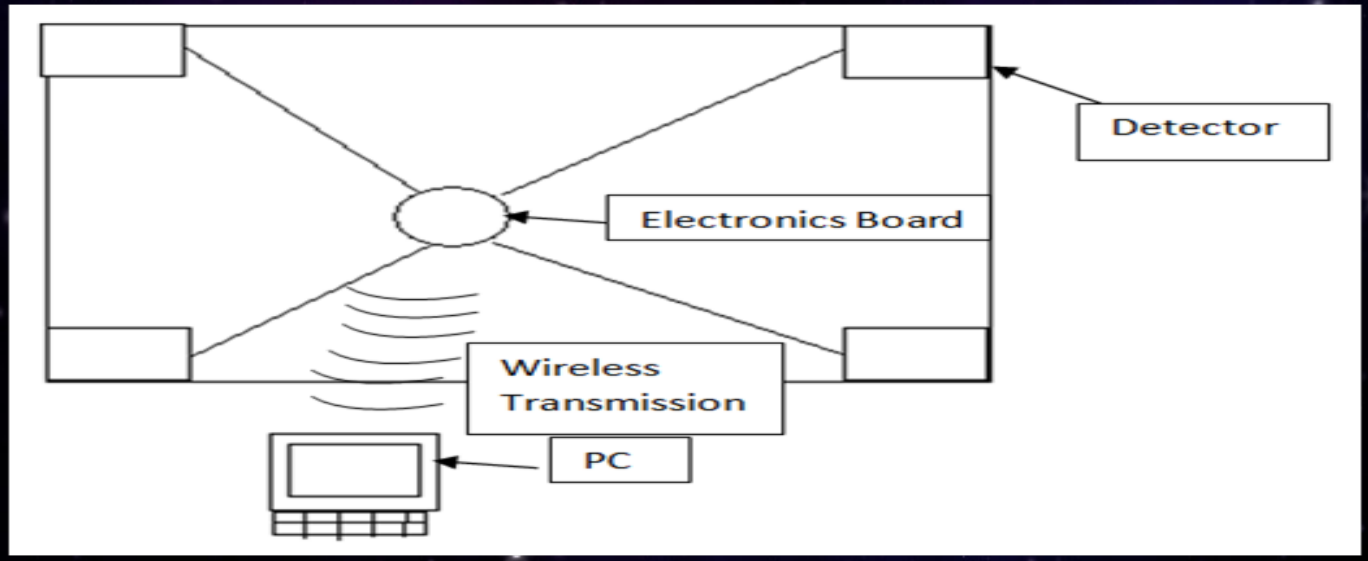
Cosmic Rays

- Ultra High Energy Cosmic Rays are sub-atomic particles with an energy band in the 10^{20} eV (~15J)
- Uncertain origins



Overview

- Cosmic Ray Showers enter earth from outer space.
- Showers are detected by Scintillators and Photomultiplier Tubes (PMT) setup.
  - Emits light when excited by radiation
  - Light is detected by PMT and amplified
  - Signal is sent to the electronics board
- FPGA board analyzes pulses from PMT and records the data on a server.



Problem Statement

- Phase I
  - the detectors will send voltage pulses through coaxial cables to an FPGA for digitization.
  - This data will be wirelessly transmitted to the kiosk.
  - Bit width reduction to make room for new inputs
  - Desired frequency of final design will be 500MHz
  - The system components will have a mounted enclosure
  - Detectors will be installed at the Challenger Learning Center
- Phase II
  - One FPGA to each scintillator
    - optically synchronized
  - New FPGA board design
    - PALS software license required

Intended Users

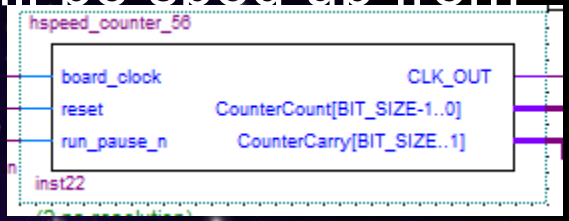
- **Intended Users**
  - Will be implemented in learning centers
    - Challenger Learning Center
    - High Schools
    - Libraries
    - Astrophysicists
- **Intended Use**
  - Capture Cosmic Ray Shower events
  - Triangulate location
  - Contribute Data to MARIACHI (Mixed Apparatus for Radar Investigation of Atmospheric Cosmic-rays of High Ionization) data sets

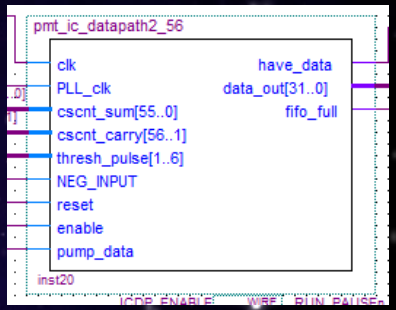
High-Speed Components and Bit-Width Reduction

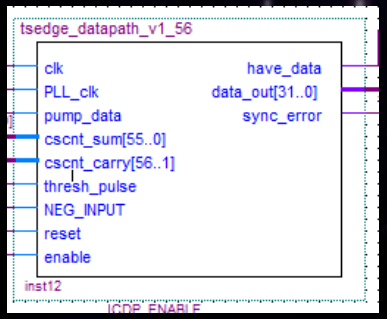
Michael Dean
Computer & Electrical Engineering

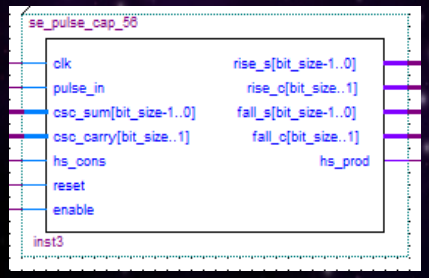
Speeding Up Operational Frequency: Components of the System

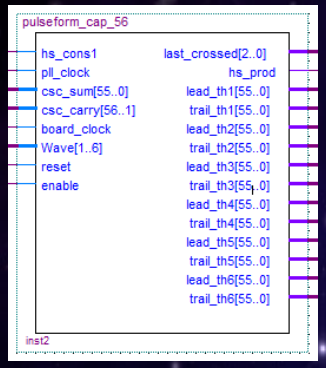
- The high-speed components in this system, those using the Phase-Locked Loop (PLL) line, will be sped up from their current 211 MHz to 500MHz
- High-speed time-counter
- Input Capture Datapaths
- Photo-multiplier Tube Pulse Digitizer
- Pulseform Capture Datapath
- Pulse Prep
- SE Pulse Cap

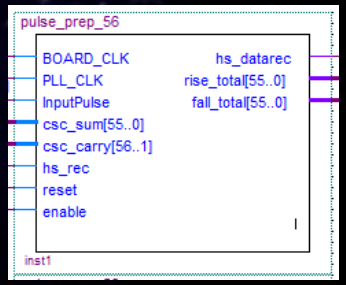












Circuit Speed Increase: Logic Locking

- In order to increase the Front-End Digitizer Module (FEDM) to an operational frequency of 500MHz Quartus' Logic Locking feature will be utilized
- This will be applied to the high-speed components to prevent Quartus from adding unneeded logic elements to the components at compile time.
- Memory on the board will also be freed up and help with the addition of more input lines.

Circuit Speed Increase: Design Process

- This phase will not be started until the FEDM code modifications to incorporate the timing-sync input datapath has been completed.
- At that point we will finish researching how to utilize Logic Lock
- Two approaches will be used:
  - Removing a few components locking them and then testing the frequency. Repeat locking a few more components at a time until the frequency is returned to 500MHz
  - If the first method doesn't work (if it does it will save significant amounts of time) the design will be broken down to the lowest levels and rebuild up to the top level with each component being logic locked

Circuit Speed Increase: Percentage Completion

Logic Lock Components: 75% of Overall Task

Subtasks: Logic Lock Goal is 0% Complete

- Research Logic Lock - 5% TBD
- Logic Lock Lowest Level Components - 25% TBD
- Test Frequency Operation Level - 10% TBD
- Logic Lock Additional Levels - 25% TBD
- Test Frequency Operation Level - 10% TBD

Integrate Into Project: 25% of Overall Task

Subtasks: Integratio Goal is 0% Complete

- Test Integration of New Frequency - 15% TBD
- Test for Errors - 10% TBD

Overall Task is 0% Complete

Circuit Speed: Risk Assessment

The Stratix II chip may overheat if the cooling system does not effectively maintain an operational temperature

Probability of this occuring: Low

Impact: This would be detrimental if the system overheated and started collecting incorrect data at a larger margin than 2ns per reading.

Countermeasures: The board will be tested in the lab to make sure it is properly cooled.

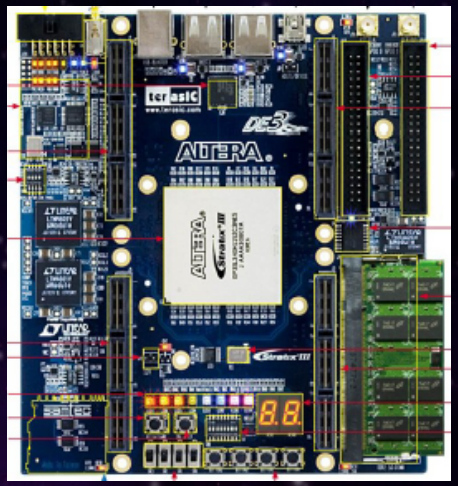
Timing Components: Purpose

- Central Timing Unit:
  - WiFi Module
    - Currently used to establish a wireless connection between the Central Server (Kiosk) and the board
  - GPS Sub-System
    - GPS Module sends a serial input stream and a timing sync reference signal to the DE3 board "real world time"
  - High Precision Oscillation (Timing Reference Board)
    - Sends a 10MHz signal to the board at the start of each run which functions as a "relative time" signal
  - FEDM Control Software (DE3 Board)
    - This is the control software which is being run on a DE3 board with a Stratix III FPGA chip. This board allows the user to interact with with custom FPGA board.

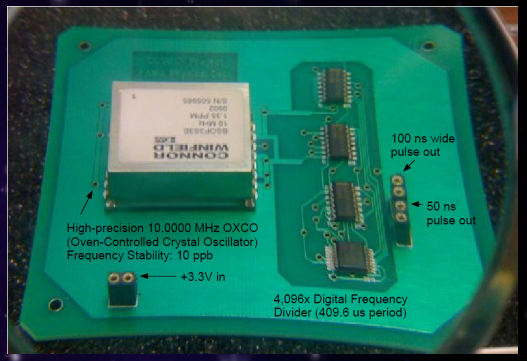
Timing Components: Setup

Below is a map of the Timing Component interconnections

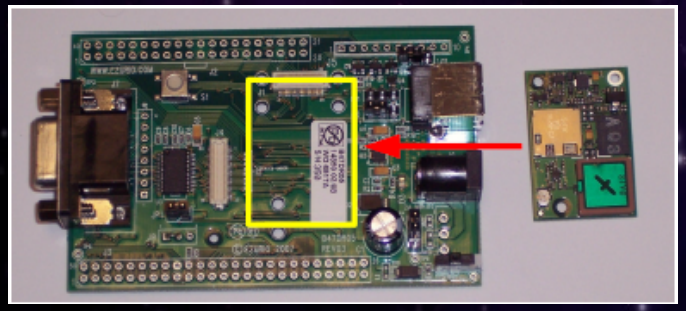
GPS Module



DE3 Board with Stratix III Chip



High-Speed Oscillator



WiFi Module

Server Kiosk

Reducing the Bit Width: Design Process

- The reduction of bit-width was done by implementing a constant value into the Verilog and VHDL code files and setting it to 56
- This is an ideal solution to the problem because possible future modifications to the bit-width can be easily changed by adjusting the value in these 6 spots rather than changing the value in 6 files at every occurance
- The files that were modified are:
  - h-speed_counter.v
  - fifo_reader.vhd
  - fifo_writer.vhd
  - cs_combine.vhd
  - se_pulse_cap.vhd
  - stream_pulse_data.vhd

Performance Assessment: After Bit-Width Reduction

- The internal timing counter was 64-bits wide, giving over 10 years data values
- This value was reduced to 56-bits and still give 4.5 years
- The system memory improvements after reduction:

Before:

- Slow Corner Fmax for high-speed counter: 211.28MHz
- Logic Utilization: 24,314 / 27,104 (90%) = 2,790 remaining
- Dedicated logic registers used: 21,878 / 27,104 (81%) = 5,226 remaining
- M512 blocks: 193/202 (96%) = 9 remaining
- M4K blocks: 144/144 (100%) = 0 remaining
- M-RAM blocks: 1/1 (100%) = 0 remaining

After:

- Slow Corner Fmax for high-speed counter: 213.13 MHz (slightly better)
- Logic Utilization: 22,007 / 27,104 (81%) = 5,097 remaining (almost 2x better)
- Dedicated logic registers used: 19,463 / 27,104 (67%) = 7,641 remaining
- M512 blocks: 188/202 (93%) = 24 remaining (more tha n 2x better)
- M4K blocks: 144/144 (100%) = 0 remaining (same)
- M-RAM blocks: 1/1 (100%) = 0 remaining (same)

Reducing Bit-Width: % Completion

Code Reduction: 80% of Overall Task

Subtasks: Code Reduction Goal is 100% Complete

• Familiarize with code - 5%	Complete	9/21/11
• Implement Global Variables - 30%	Complete	10/5/11
• Recreate Newly Sized Component Blocks - 30%	Complete	10/19/11
• Re-wire and Re-label Components - 10%	Complete	10/23/11
• Debug and Test for Completion - 5%	Complete	11/2/11

Add Additional Input Line: 20% of Overall Task

Subtasks: Additional Input is 100% Complete

• Add Additional Input VHDL Code - 10%	Complete	11/2/11
• Test for Errors - 10%	Complete	11/2/11

Overall Task is 100% Complete

ICPDs - Risk Assessment

The input capture datapath may malfunction and fail to transmit data should something cause the board to shake/dislodge and damage its internal components (from events such as a hurricane, tornado etc.)

Probability of this occuring: Low

Impact: The ICDP is essential to transmitting collected data through the system and to ultimately to the servers. Should it malfunction this would invalidate the data collected by the board.

Countermeasures: The board has been undergoing test runs to collect data and has proven to be effective so far. Should the input path fail once installed it won't have any fallbacks and will have to be taken out and evaluated for the source of the error.

Timing-Sync Datapaths: VHDL

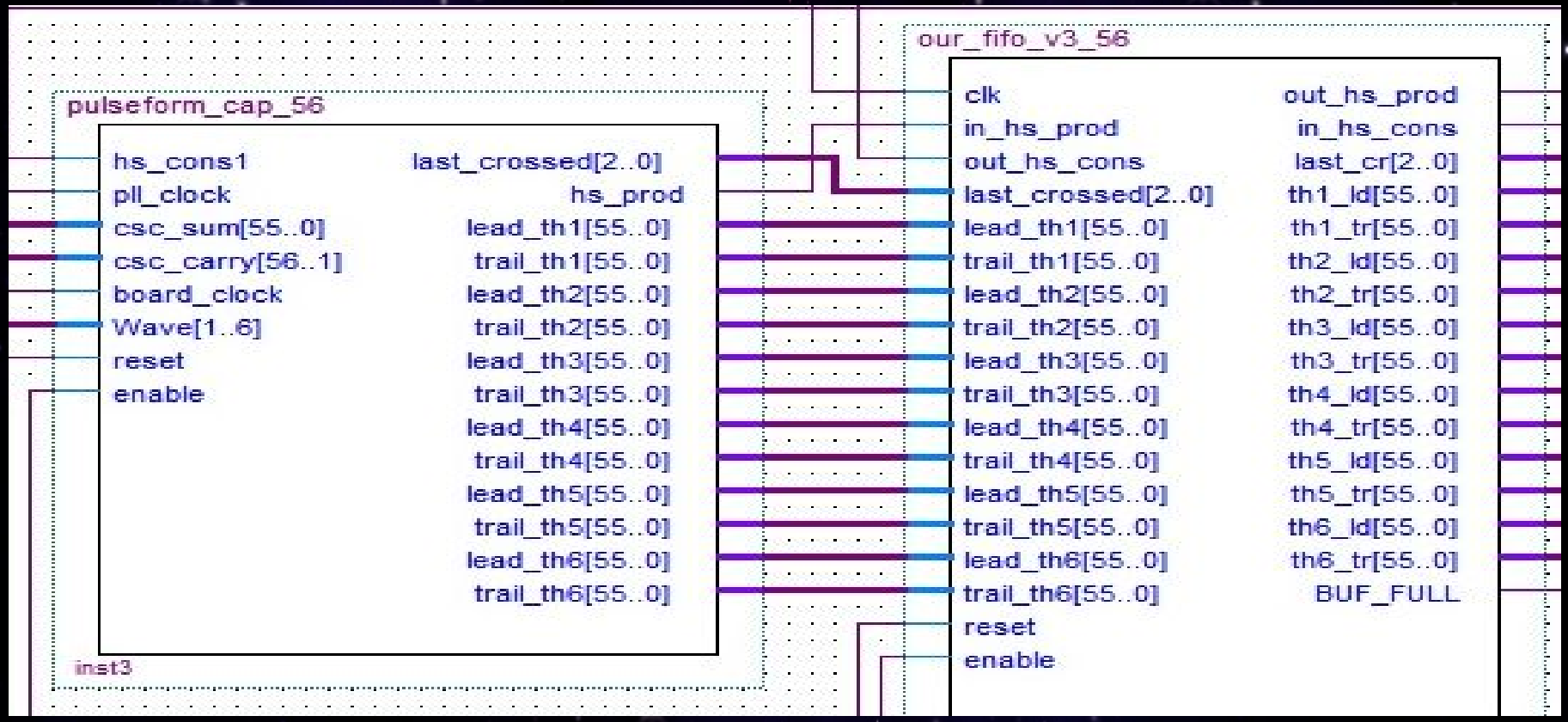
Aarmondas Walker
Computer Engineering

Timing-Sync Datapaths: VHDL

The TSDP is being modified to disregard the voltage thresholds 2-6. It is now only concerned with the first voltage threshold. This module will only be triggered by the rising edge of the threshold.

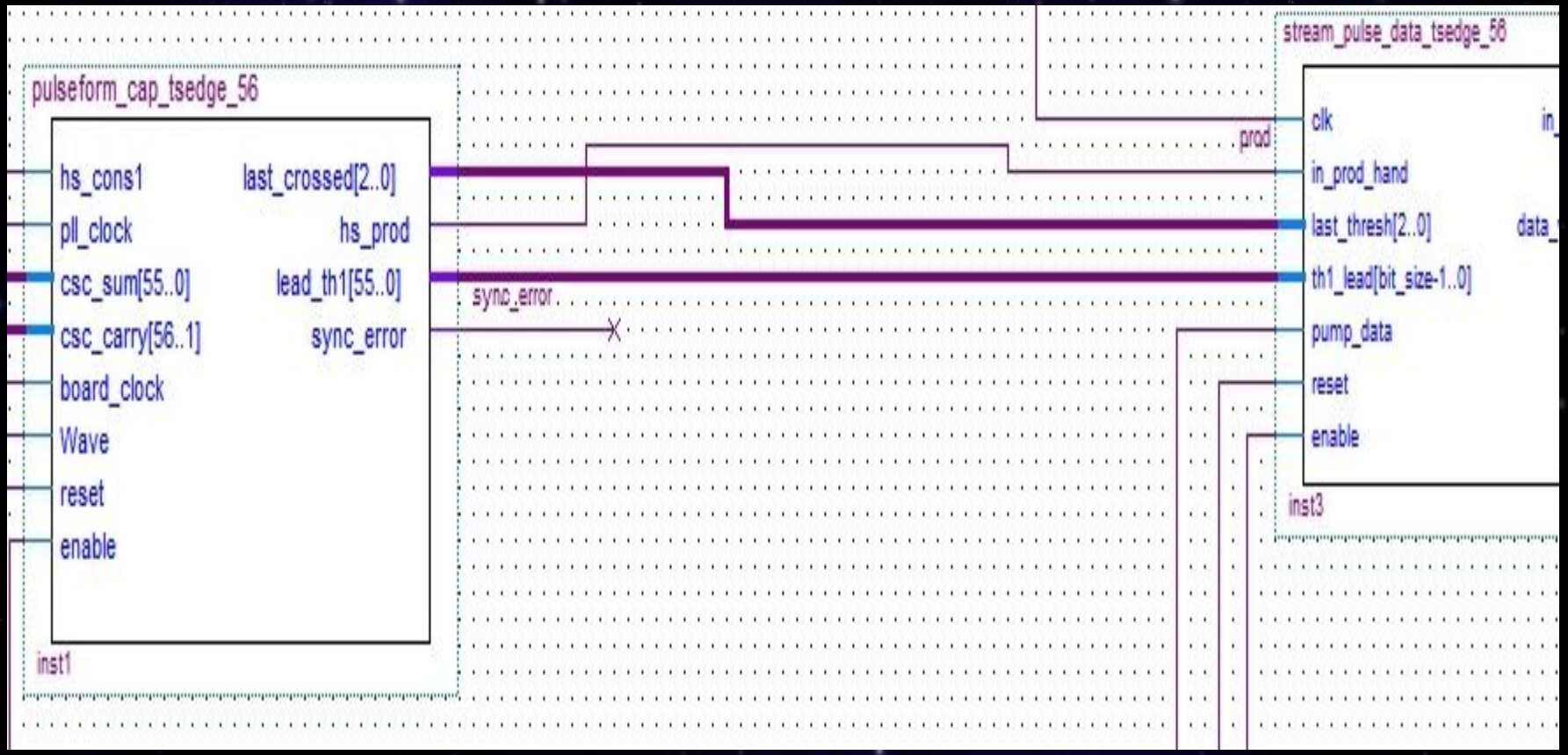
Timing-Sync Datapaths: VHDL

Before Modifying



Timing-Sync Datapaths: VHDL

After Modifying



Front end digitizer module(FEDM)

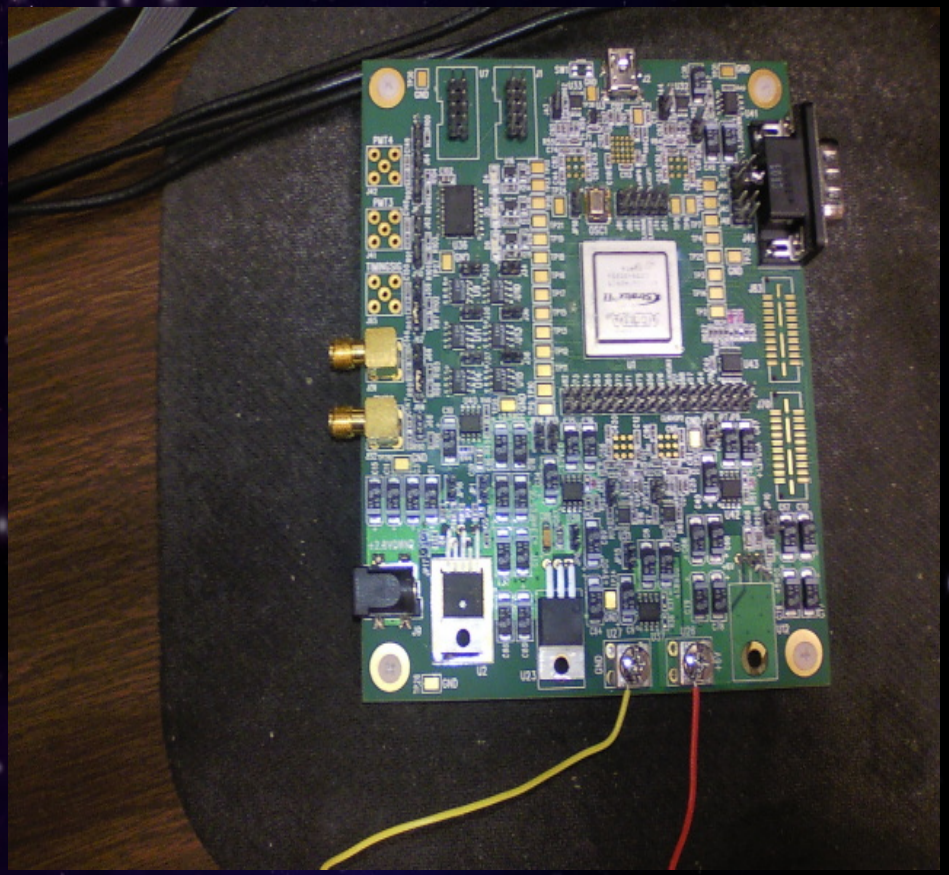
Juan Calderin
Computer Engineering

Front End Digitizer Module

Purpose:

To digitalize the analog signals from the cosmic ray detectors and have them ready for the server to process them.

Mainly written in C and VHDL



Front End Digitizer Module (updates)

Task: Add 2 new Parallel Input/Output (PIO): timing sync data path and timing sync control.

Approach:

1) Specify what each bit will be in the control PIO and the bit-width size of the data PIO.
2) Add the new PIO to the SoPC design.
3) Design the driver code in 'C'.

Front End Digitizer Module

Specifying the bit-width size

- Timing Sync Data Path PIO will have 32 bits for the data.

- Timing Sync Control Bits:

```
#define   TSDP_RESET_MASK          (1<<0)     //  TSDP_RESET          is bit  0 (0x001).
#define   TSDP_ENABLE_MASK         (1<<1)     //  TSDP_ENABLE         is bit  1 (0x002).
#define   TSDP_PUMPDATA_MASK       (1<<2)     // TSDP_PUMPDATA        is bit  2 (0x004).
#define   TSDP_HAVEDATA_MASK       (1<<3)      // TSDP_HAVEDATA              is bit  3 (0x008).
#define   TSDP_SYNC_ERROR_MASK     (1<<4)      // TSDP_HAVEDATA       is bit  4 (0x010).
```

Front End Digitalizing Module

Designing the driver

- Modeled after existing input capture data path driver (icdp.c)

- New source file: "tsdp.c"

```
void    tsdp_reset(void);       // Resets the state
int     tsdp_have_data(void);  // TRUE (1) if it has data to send
void    tsdp_run(void);     // Enables timing-sync-capture datapath
void    tsdp_pause(void);           // Pauses the operation
void    tsdp_handle_have_data (void);  // Calls tsdp_have_data isr
void    tsdp_handle_sync_error (void);   // in case of sync errors
```

- One generic driver

- Using one PIO instead of two

Front End Digitalizing Module

Schedule

- Driver design (12/16/11)
- Adding new PIO to SoPC design (12/16/11)
- Testing new timing PIO (1/14/12)

Risk Assessment

- Running out of space in the buffer (Probability: Moderate)

- Interrupts interrupting each other (Probability: Low)

Central Server

Purpose: to process and graphically display the data coming wirelessly from the FPGA.
Written in Python
The server will be running in the kiosk computer located in the Challenger Learning Center.

Central Server (updates)

Tasks:

- **Information Display**:
  We can use the VPython libraries for 3D display.
  Integrate it with Google Sky using the Google Earth API.

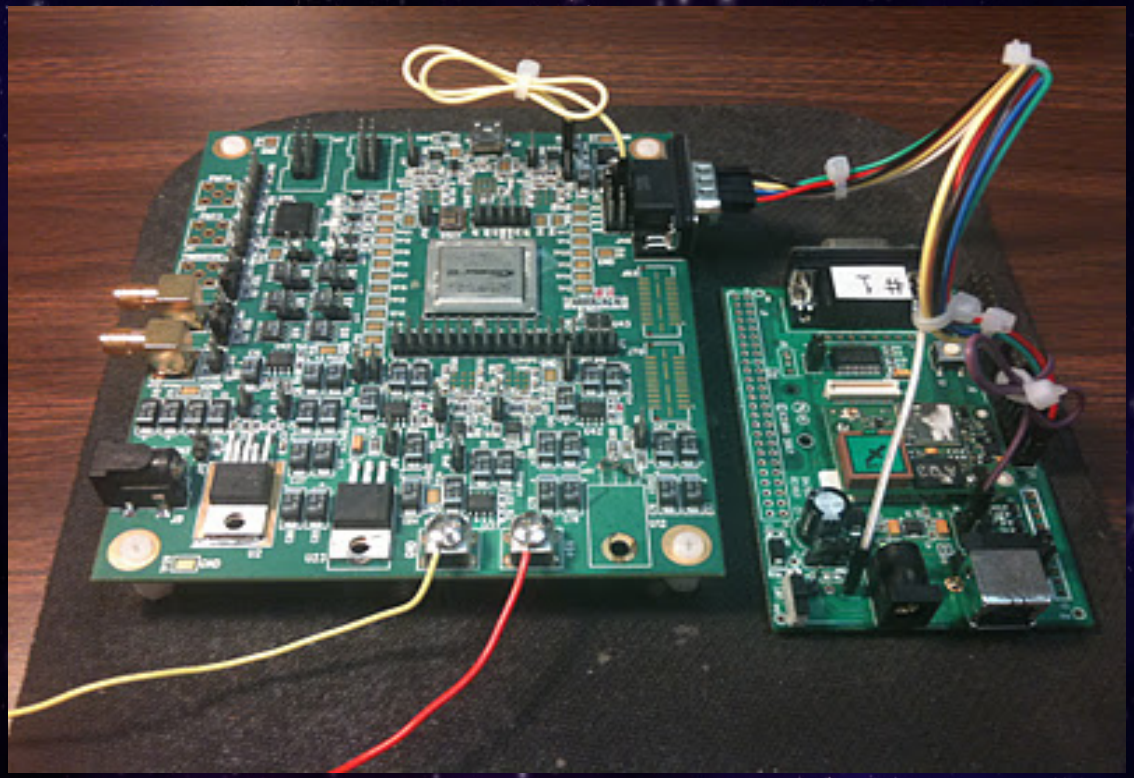
Risk Assestment

- **Google Earth or Sky Map being down (Probability: Low)**
  - Use the new map cache feature

Power Supply

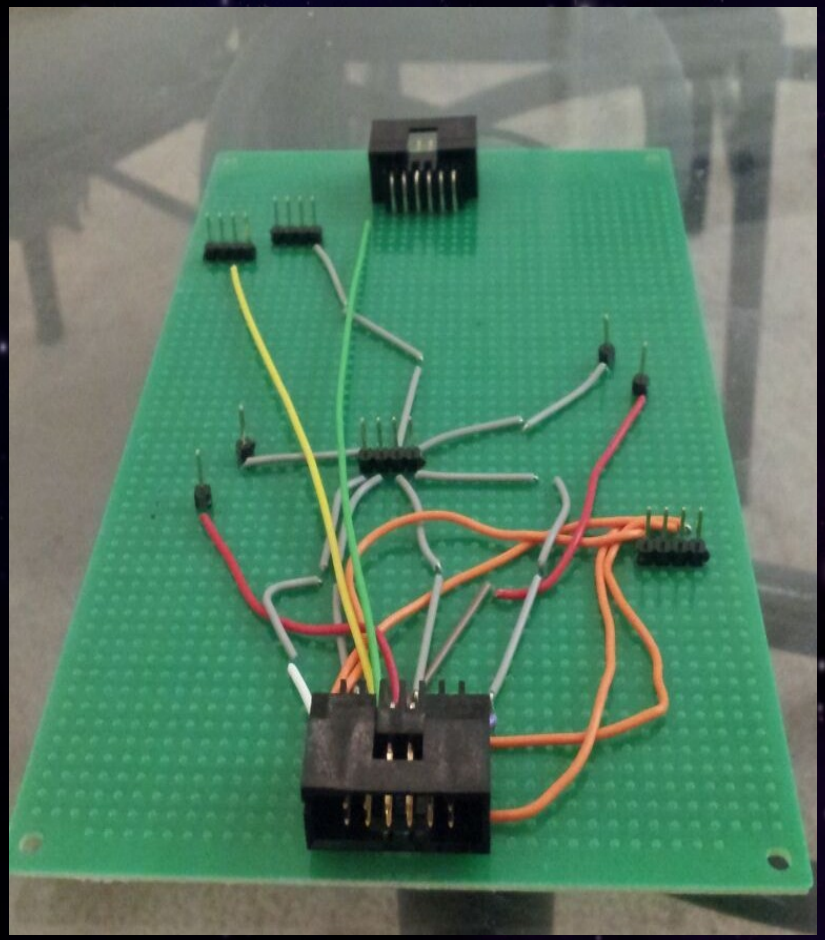
Samad Nurideen
Electrical Engineering

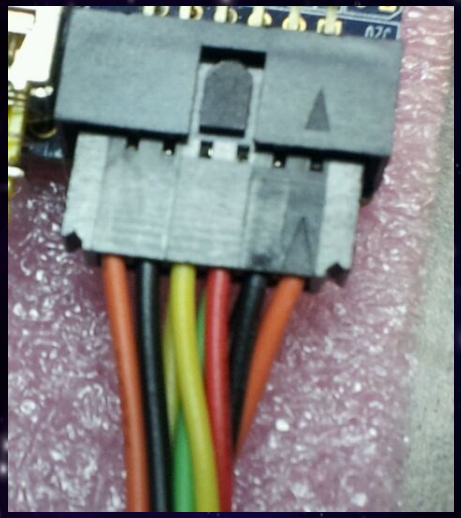
FEDM + Wireless Board



CTU

Powering Components





Detectors

Finding a Battery

- Detector's Input Voltage (12V, Nominal)
- Detector's Power Consumption (250mW)
- Detector's Maximum Current Drain (21mA)
- Expected Battery life: 3 Weeks/504 hrs)

Detectors

Battery For Detector

Lithium Ion Rechargeable Charger

Battery Pack (2): 12V, 4.5Ah

Battery

Detectors

Calculations For New Battery

4.5Ah/.021A= 214.2857hrs

214.2857hrs/168hrs= 1.27 Weeks

Battery in Parallel

9Ah/.021A= 428.57hrs

428.57hrs/168hrs= **2.55 Weeks**

Power Supply % Completion

Power Supply – 80% of Overall Task Goal

Subtasks:

Power FEDM – 10%	Complete	10/5/11
Power CTU – 10%	Complete	10/19/11
Power both CTU and FEDM – 70%	0%	
Provide Power for detectors – 10%	0%	

POWER SUPPLY GOAL IS 20% COMPLETE

Battery – 20% of Overall Task Goal

Subtasks:

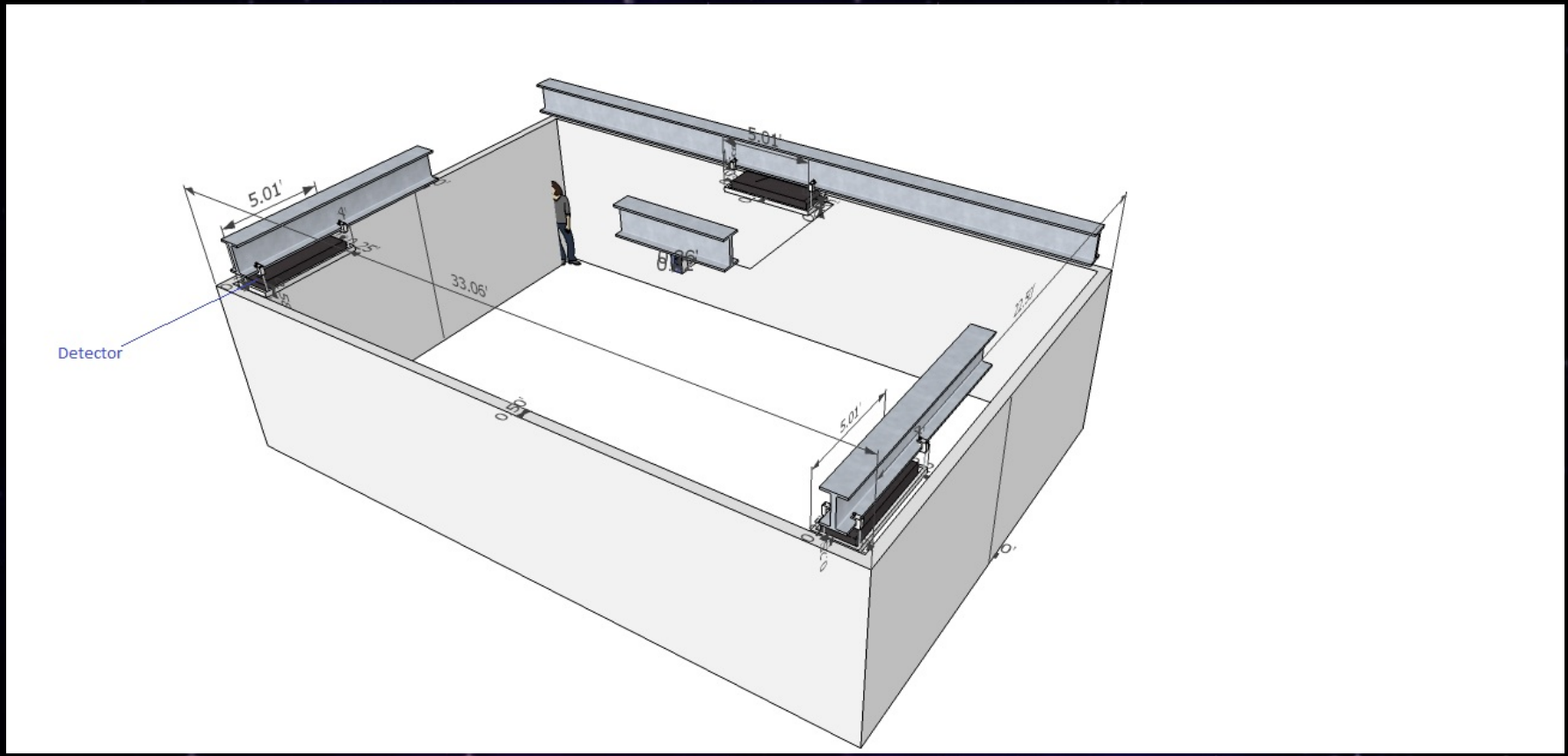
Research – 30 %	Complete	10/20/11
Order Parts – 10%	5%	
Implement – 40%	10%	
Test – 40%	10%	

55 % OF BATTERY GOAL IS COMPLETE

Structural Support
&
Enclosure Design

Brian Kirkland
Mechanical Engineering

Structural Support



Scintilator-detector measurements:

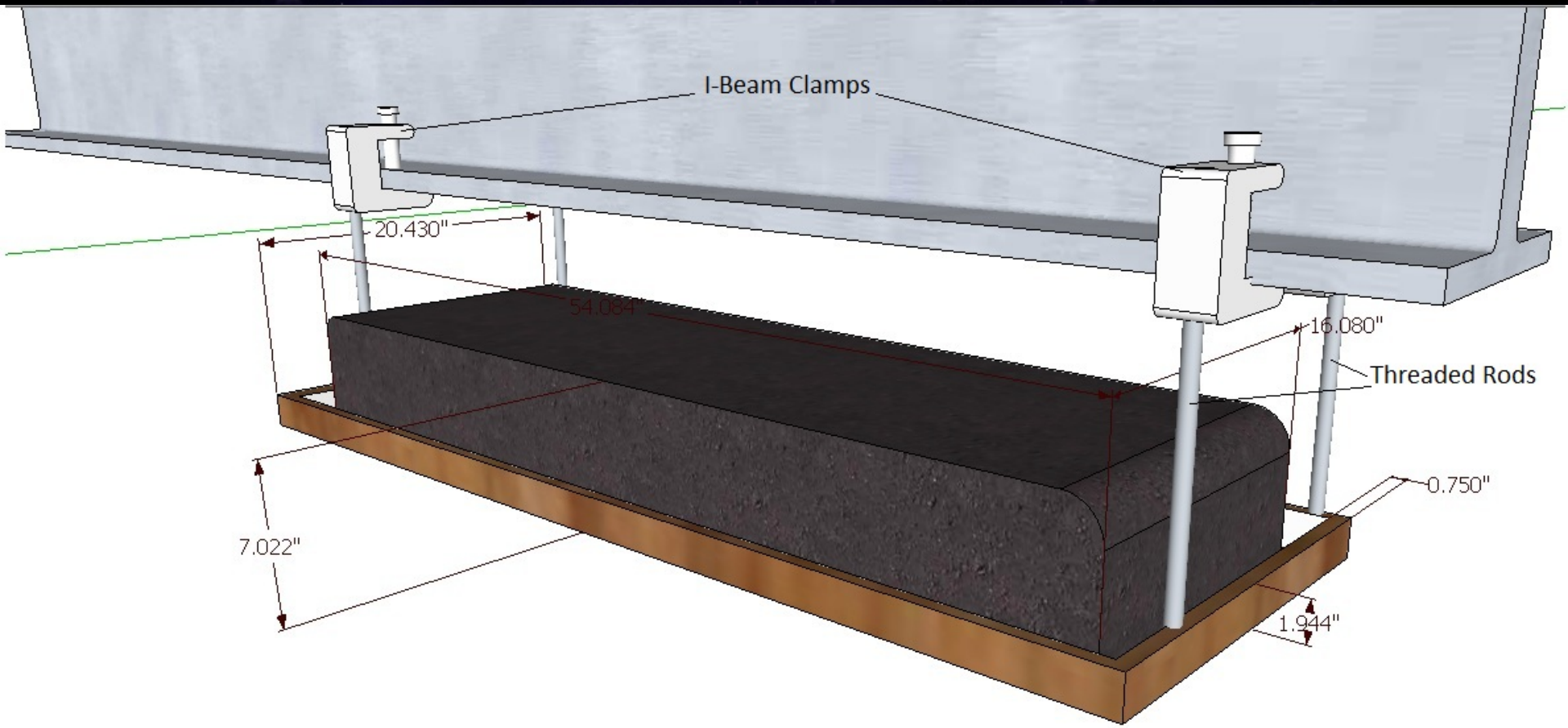
Dimensions:~54"X16"X7"|

Weight ~25lbs

CLC Safety Rules:

1. Suspended objects must be attached to structure
2. Wires/cables must be in a conduit

Structural Support



Structural % Completion

Scintillator Support – 75% of Overall Task Goal

Subtasks:

• Scintillator Measurement – 10%	Complete 10/07/11
• Room Measurement– 10%	Complete 10/14/11
• Fastening Method Analysis – 50%	Complete 11/05/11
• Part Ordering-20%	TBD
• Design Implementation – 10%	TBD

70% OF OVERALL STRUCTURAL SUPPORT GOAL COMPLETE

Structural Components

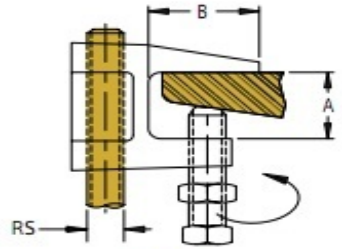
Caddy Beam Clamp 3/8" Rod Size $2.39 (ea.) Quantity 16 Supplied By Grianger
http://www.grainger.com/Grainger/CADDY-Beam-Clamp-1RUY3?cm_sp=IO-_-IDP-_-RR_VTV70300505&cm_vc=IDPRRZ1

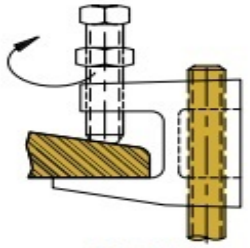
Detector Shelving 3 pc $282 Supplied By Metal By The Inch
https://www.metalbytheinch.com/index.php?shopping_cart=yes

Threaded Rods 304 SS 3/8"-16 6' $8.89 (ea.) Quantity 16 Supplied by Grainger
http://www.grainger.com/Grainger/Threaded-Rod-4RDJ3?Pid=search

Hex Nut, 3/8"-16 PK 100 $6.29 Supplied By Grainger
http://www.grainger.com/Grainger/Hex-Nut-3HEF1?cm_sp=IO-_-IDP-_-BTM_BTB05209020&cm_vc=IDPBBZ2

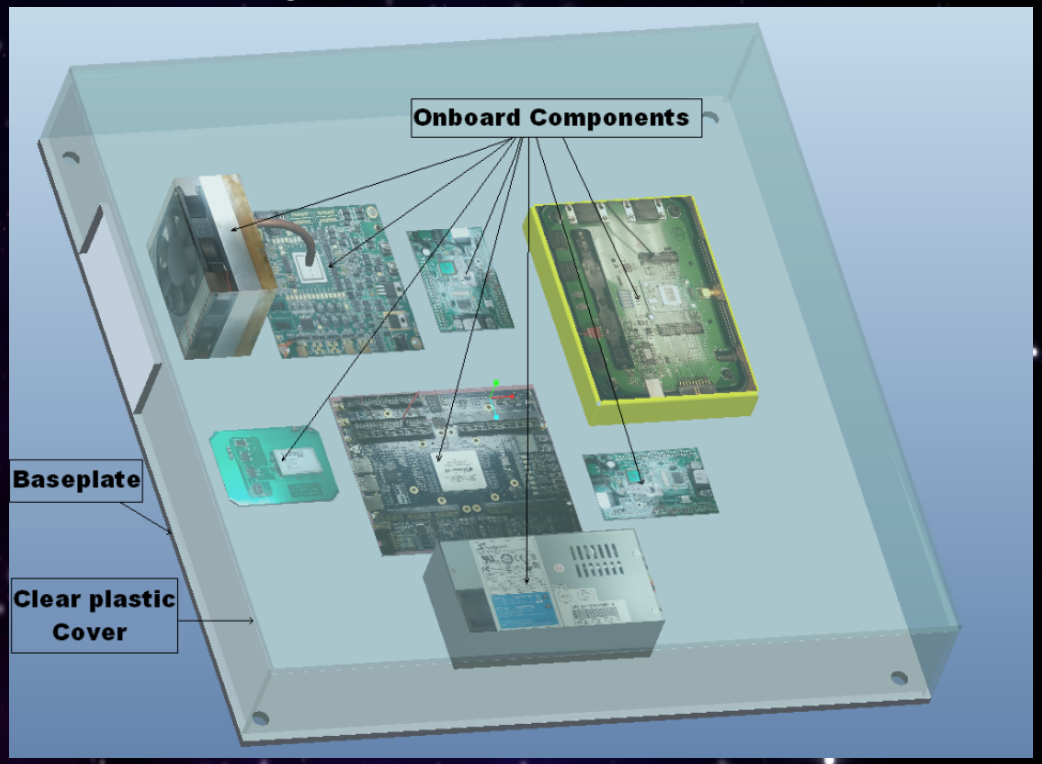
Split Lock Washer PK 100 $12.30 Supplied By Grainger
http://www.grainger.com/Grainger/Split-Lock-Washer-1NY99?cm_sp=IO-_-IDP-_-BTM_BTB05209020&cm_vc=IDPBBZ2





Enclosure: Summary

- Need an enclosure to house electronic components.
- Previous design aluminum plate
  - Excessive cost
  - Not feasible for mass production
  - Can be made better by proper material selection



Enclosure Basics: Recap

- **Enclosures are built to protect objects from**
  - **Physical Shock/Perturbations**
    - **Flying projectiles**
    - **Dropping**
  - **Foreign object debris**
    - **Dust**
    - **Dirt**
    - **Water**

Enclosure System

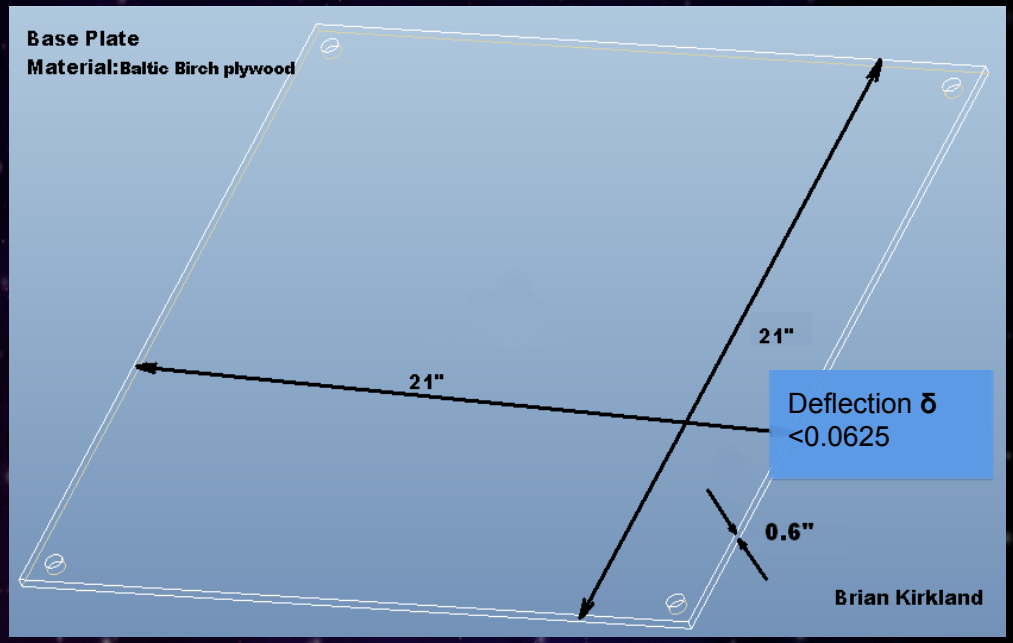
- **The enclosure for this system is comprised of two separate components**
  - **Base plate**
  - **Cover**
- **The base plate previous design**
  - **Aluminum plate**
    - **Too heavy**
    - **Too expensive**

Enclosure system Cont

- **The enclosure system will be hung from the ceiling**
  - **Structural support system**
    - **Max capacity 2000 lbs**
      - **Design panel with max weight of 500 lbs for safety factor of 4**
- **Clear cover**
  - **Made of Clear plastic**
  - **Can comprise free materials from local home improvement stores**
    - **Zero cost increse**
    - **free machining at Engineering campus**
  - **Allow view of components working**
    - **LED's blink when data is being transferred or received**
    - **Cooling system will have moving parts**

Base Plate FCOFV

- **Function**
  - Panel
- **Constraints**
  - Length/Width L = 21”
  - Deflection δ < 0.0625“
  - Mass < 500 lbs
  - Aesthetic finish
- **Objective**
  - Minimize cost
- **Free variables**
  - Material Selection
  - Thickness



Solving for Objective

- **Main equations – Main relation**

$$C = m * C_m$$

- **(1) cost/mass**

$$m = \rho * A * t$$

- **(2) mass/density**

$$\delta = \frac{L^3 * F}{C_1 * E * I}$$

- **(3) deflection/modulus**

$$I = \frac{L * t^3}{12}$$

- **(4) moment of inertia**

Solving for objective cont.

- **Worked equations - Process**

$$\delta = \frac{L^3 * F}{C_1 * E * \frac{L * t^3}{12}}$$

$$t = \left(\frac{12 * F * L^2}{C_1 * E * \delta}\right)^{\frac{1}{3}}$$

$$C = \rho * A * t * C_m$$

$$C = \rho * A * \left(\frac{12 * F * L^2}{C_1 * E * \delta}\right)^{\frac{1}{3}} * C_m$$

  - **(5)-substituting I from (4) into (3)**
  -
  - **(6)-solving (5) for thickness**
  -
  - **(7)-substituting (2) into (1)**
  -
  - **(8)-substituting (6) into (7)**

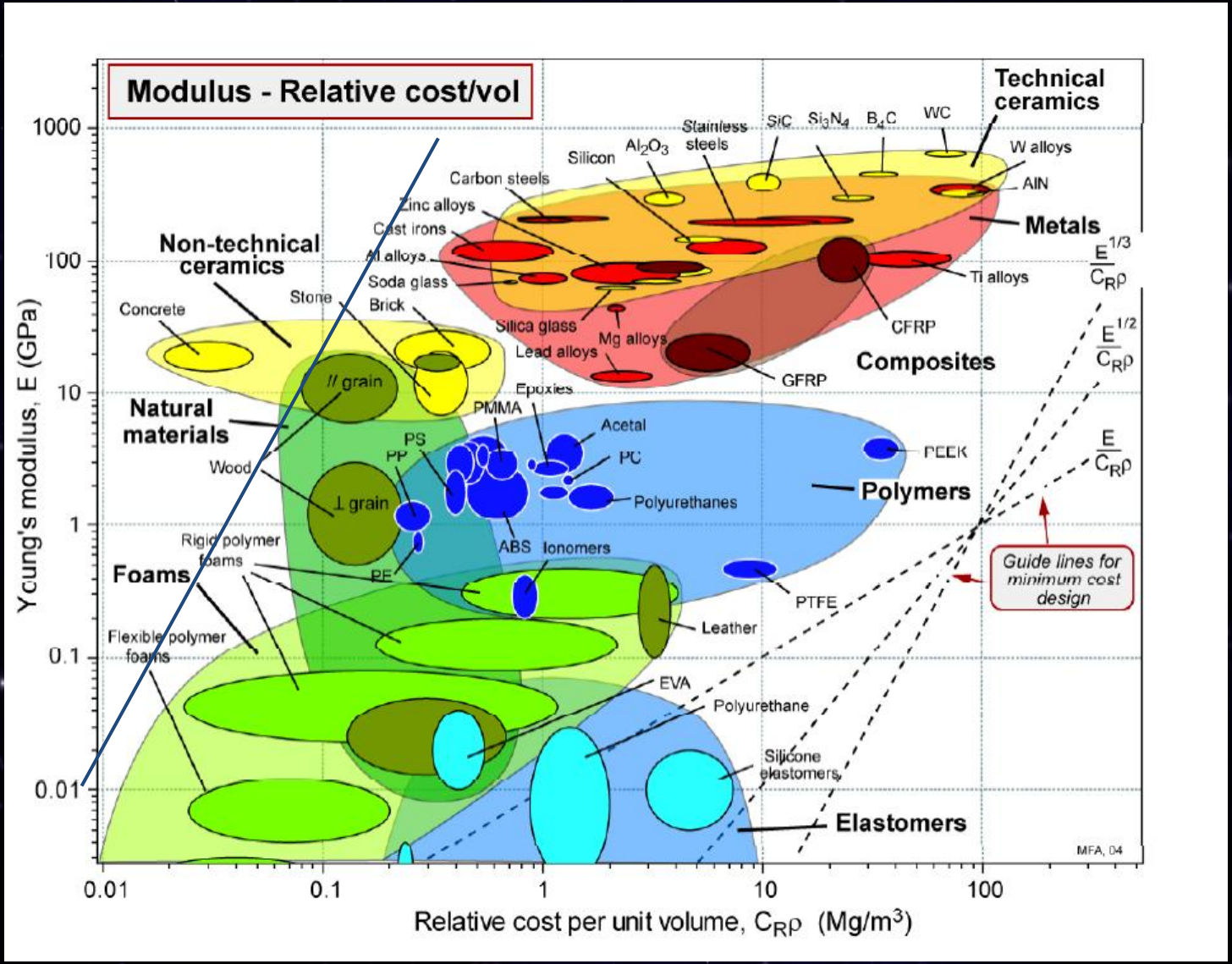
Solving For objective Cont.

- Material Index
- Final objective equation

$$M = \frac{E^{\frac{1}{3}}}{\rho * C_m}$$

$$C \geq \frac{1}{M}\left(\frac{12 * F * L^2}{192 * \delta}\right)^{\frac{1}{3}}$$

Material Selection chart



Sizing Component

- Need to substitute real world values not estimates
  - Using Thickness equation

$$t = \left(\frac{12 * F * L^2}{C_1 * E * \delta}\right)^{\frac{1}{3}}$$

  - Plug in Values; value of F, δ, and L obtained from constraints; Value of E found online it is the modulus for Birch Plywood, C1 found in Ashby's textbook

$$t = \left(\frac{12 * 2224.02\,N * 0.5334^2\,m}{192 * (8.2737 * 10^9\,Pa) * (1.588 * 10^{-3} m)}\right)^{\frac{1}{3}}$$

$$t = 0.014439\,m \approx 0.5865"$$

Sizing component cont.

- Solving for the Mass

$$m = \rho * A * t$$

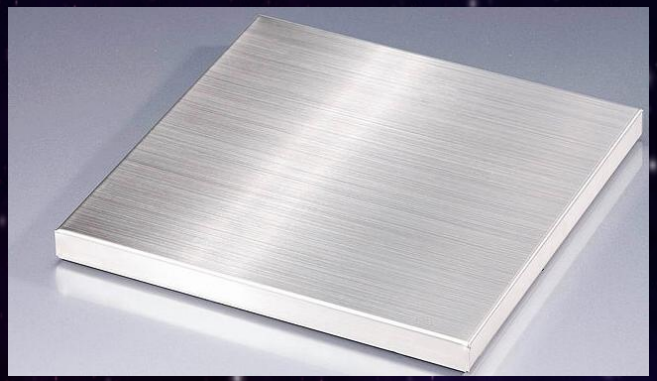
- Plugging in values for ρ(found online), A(L2), and t that was just calculated
- Gives a final value of

$$m = 528.609 \ \frac{kg}{m^3} * 0.284516 \ m^2 * 0.014439 \ m$$

$$m = 2.172 \ kg \ll 500 \ lbs$$

Material Comparison

- Previous design
  - Aluminum
    - Heavy
    - Expensive
      - Material
      - Machining
- Modified design
  - Baltic Birch Plywood
    - Light
    - Inexpensive
      - Material
      - Machining



Material Choice: Conclusion

- Redesign helped
  - Save project money
    - Material cost
    - Machining cost
  - Improve Mass production feasibility
  - Reduce mass
  - Improved knowledge of material selection process

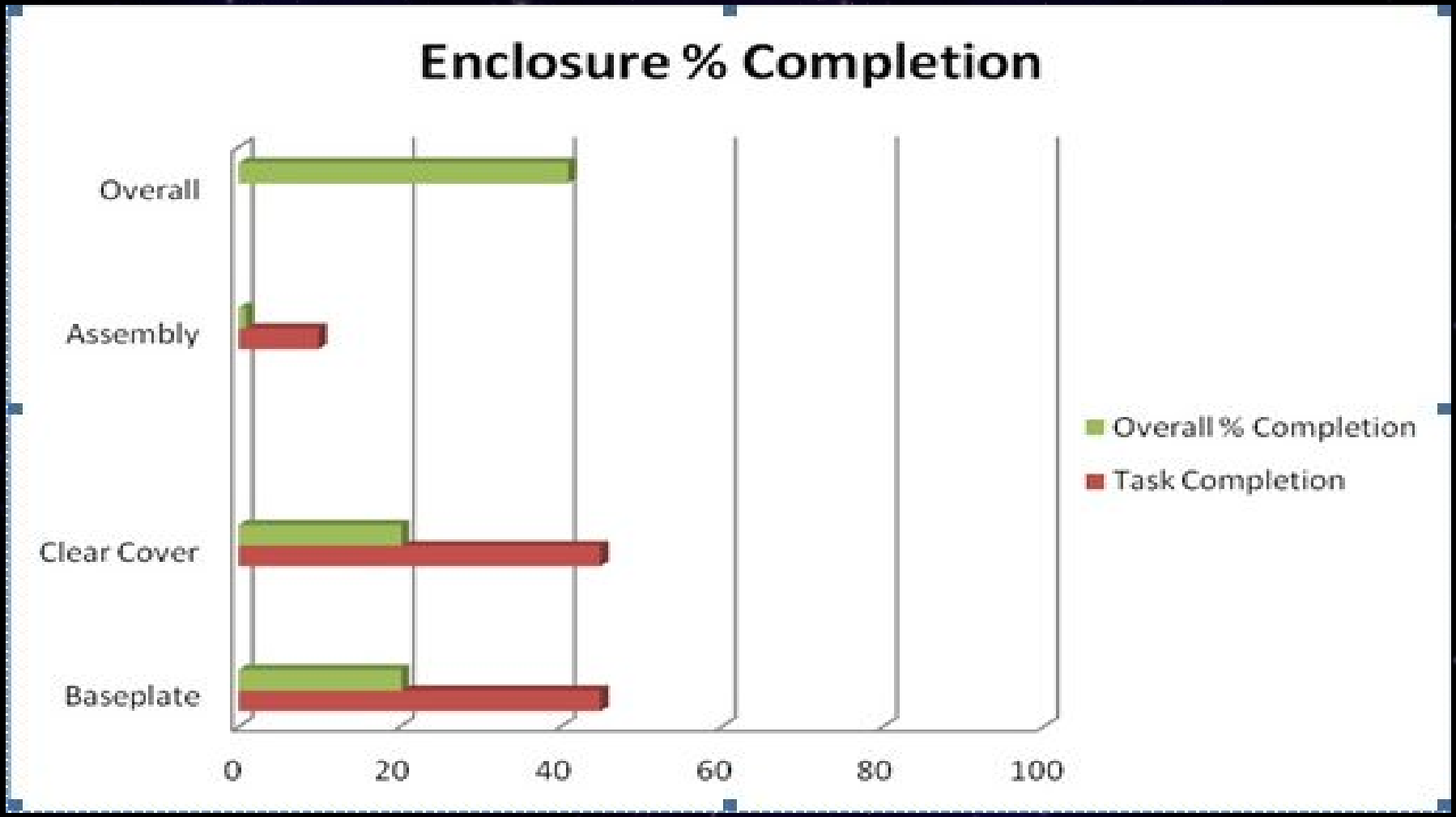
Enclosure % Completion

Subtasks:

- **Base plate:** 45% — 21%
  - Designing : 31.5%
  - Machining: 13.5%
- **Clear Cover:** 45% — 20%
  - Designing: 27%
  - Machining: 9%
  - Fabrication: 9%
- **Assembly**: 10 % — 0%
  - Fabrication: 10%

41% OF OVERALL ENCLOSURE GOAL COMPLETE

Enclosure % Completion (cont)



Cooling System

George Chakhtoura
Mechanical Engineering

Cooling System

1. The cooling system level design that will be implemented will use Peltier Heat Transfer method.
2. With a simple redesign of the current system, the new operating temperature of the Stratix II chip will be 0^{o}C +/- 2^{o}C.
3. Replacing the aluminum block with a copper rod, the higher thermal conductivity of 401 W/m*K will create a greater heat transfer rate from the chip.
4. Using a full copper heat sink and fan set up will remove the highest amount of heat while continuing to be cost effective.
5. Covering the copper rod with a Silicone Adhesive will prevent the condensation build up on the pipe and chip.

Cooling System Cont...

1. Copper has 2X the thermal conductivity of Aluminum and 3X that of Stainless Steel, thus the material change for the heat pipe and fins.

2. The new copper fin mounted fan will consume an equal amount of power with a greater air flow and RPM rate.

$Q=k*a*(T_{hot}-T_{cold})/d$

Established Heat Rate (from current system)	Q= 126.563 W
Cross Sectional Area	a= 5cm^2
Rod Length	d= 8.4cm
Thermal Conductivity of Copper	k= 401 W/m*K
Running Temperature (T_{hot})	T_{hot}= 53ºC (326K)
Desired Running Temp(T_{cold})	T_{cold}= 0ºC (273K)

Cooling System Components

The most efficient and cost effective items that are planned to be purchased are listed below:

Copper Alloy 110 3/4" diameter X 1' Length $37.75 Supplied by Grainger
http://www.grainger.com/Grainger/Rod-Stock-2ABA9?Pid=search

Ultra 120mm CPU Cooler $9.97 Supplied by CompUSA
http://www.compusa.com/applications/searchtools/item-details.asp?EdpNo=4662521&csid=_21

RTV Silicone Adhesive Sealant $3.49 Supplied by Ebay
http://www.ebay.com/itm/Permatex-Clear-RTV-Silicone-Adhesive-Sealant-/230573429405?pt=Motors_Automotive_Tools&vxp=mtr&hash=item35af3f529d#ht_500wt_1054

Cooler Master Thermal Compound $7.99 Supplied by CompUSA or Ebay
http://www.compusa.com/applications/SearchTools/item-details.asp?EdpNo=3071621&CatId=503

Cooling % Completion

Subtasks:

Temperature Measurements of Chip and Board –5%	Complete	11/07/11
Physical Measurements of all Boards – 5%	Complete	10/20/11
Peltier cooler, fins, and fan cad design – 15%	Complete	11/08/11
Solve Condensation Issue –10%	Complete	11/08/11
Provide heat equations showing chip temp – 30%	Complete	11/28/11
Order correct size peltier cooler, fins and fan –5%	0%	
Connect cooling system to structure–5%	0%	
Test for Issues–25%	0%	

65 % COOLING SYSTEM GOAL IS COMPLETE

Risk Assessment: Cooling System

The copper rod connecting the Peltier cooler to the Stratix II chip could become dislodged if something were to damage the enclosure

Probability of this occuring: Low

Impact: If the cooling system malfunctions, the overheating will cause a system reboot and coorupted data.

Countermeasures: The cooling system will be mounted and supported inside the enclosure to provide additional stability.

General Information

Aarmondas Walker
Computer Engineering

Brian Kirkland
Mechanical Engineer

Expected Deliverables

Phase I:

- COSMICi System will detect UHECR from at least 3 scintillator devices
- The system will operate at a frequency of 500mhz
- The direction and source of the cosmic ray shower will be displayed to the user in the kiosk computer in the form of a sky map (possibly physics dept. task).
- A power source will be configured to supply all the components
- An enclosure will protect the circuit boards
- A Cooling System will maintain the FPGA chip at 0 C and the circuit boards at room temperature
- A structural design will support the scintillator-detectors and the enclosure

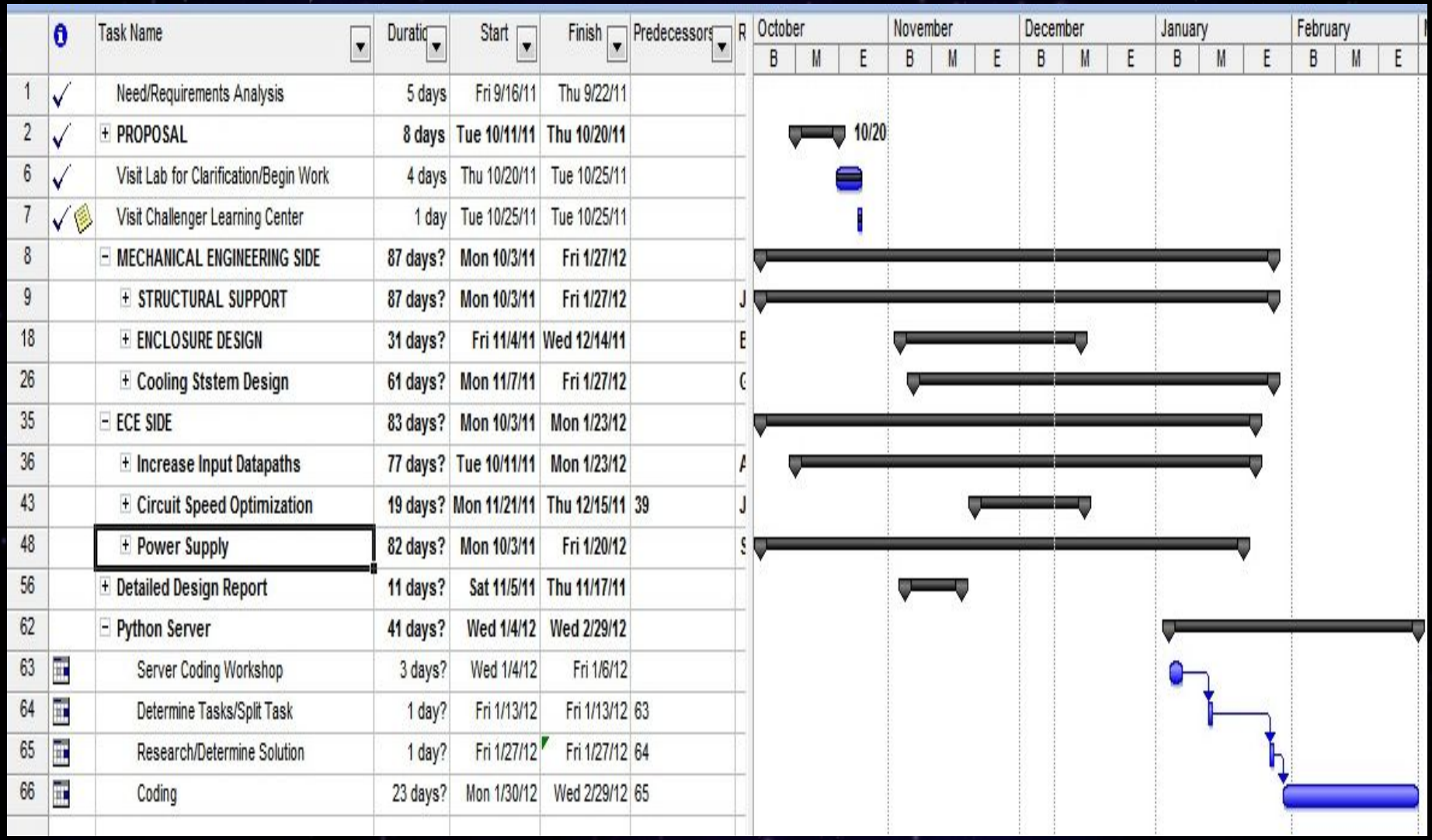
Budget

D. Expense	Quantity	Unit Price $	Total $
Equipment			
Structural Support			
Beam Clamp 3/8”	16	2.39	38.24
Threaded Rod 3/8”	16	8.89	142.24
Hex Nut Full 3/8” 100PK	1	6.28	6.28
Lock Washer 3/8” 100 PK	1	12.30	12.30
Detector Mounting Tray	3		282
Cooling System			
Copper Rod	1	37.75	37.75
Copper Fin & Fan	1	9.97	9.97
Thermal Paste	1	7.99	7.99
Silicone Sealant	1	3.49	3.49
Enclosure			
Acrylic Cover	1	68.57	68.57
Aluminum Base Plate	1	172.95	172.95
System Network			
Battery	2	59.95	119.90
Battery Charger	1	23.95	23.95
14 Gauge 100'	1	26.97	26.97
Total Equipment Cost			952.60
Total Project Cost			**952.60**

Overall Risk Assessment

- Technical Risks
  - Structural System Malfunction
  - Datapath Malfunction
  - Operational Frequency Issues
- Schedule Risks
  - Datapath
  - Enclosure Completion
- Budget Risks
  - Underestimation of Costs/Parts
  - Not Enough Funding
- Other Risks
  - Engineers Getting Sick
    - Hindering Completion of Portion
  - Engineers Dropping Out of Project

Gantt Chart - Update



	Task Name	Duratio	Start	Finish	Predecessors	R
1	Need/Requirements Analysis	5 days	Fri 9/16/11	Thu 9/22/11		
2	PROPOSAL	8 days	Tue 10/11/11	Thu 10/20/11		
6	Visit Lab for Clarification/Begin Work	4 days	Thu 10/20/11	Tue 10/25/11		
7	Visit Challenger Learning Center	1 day	Tue 10/25/11	Tue 10/25/11		
8	MECHANICAL ENGINEERING SIDE	87 days?	Mon 10/3/11	Fri 1/27/12		
9	STRUCTURAL SUPPORT	87 days?	Mon 10/3/11	Fri 1/27/12		J
18	ENCLOSURE DESIGN	31 days?	Fri 11/4/11	Wed 12/14/11		E
26	Cooling Ststem Design	61 days?	Mon 11/7/11	Fri 1/27/12		C
35	ECE SIDE	83 days?	Mon 10/3/11	Mon 1/23/12		
36	Increase Input Datapaths	77 days?	Tue 10/11/11	Mon 1/23/12		A
43	Circuit Speed Optimization	19 days?	Mon 11/21/11	Thu 12/15/11	39	J
48	Power Supply	82 days?	Mon 10/3/11	Fri 1/20/12		S
56	Detailed Design Report	11 days?	Sat 11/5/11	Thu 11/17/11		
62	Python Server	41 days?	Wed 1/4/12	Wed 2/29/12		
63	Server Coding Workshop	3 days?	Wed 1/4/12	Fri 1/6/12		
64	Determine Tasks/Split Task	1 day?	Fri 1/13/12	Fri 1/13/12	63	
65	Research/Determine Solution	1 day?	Fri 1/27/12	Fri 1/27/12	64	
66	Coding	23 days?	Mon 1/30/12	Wed 2/29/12	65	

Completed Tasks - ECE

35		ECE SIDE	83 days?	Mon 10/3/11	Mon 1/23/12	
36		Increase Input Datapaths	77 days?	Tue 10/11/11	Mon 1/23/12	
37	✓	Review current code	9 days	Tue 10/11/11	Fri 10/21/11	
38	✓	Creat plan to decrease width	3 days	Fri 10/21/11	Tue 10/25/11	
39	✓	Decrease Width	4 days	Wed 10/26/11	Mon 10/31/11	38
48		Power Supply	82 days?	Mon 10/3/11	Fri 1/20/12	
49	✓	Provide Power for FEDM	3 days	Mon 10/3/11	Wed 10/5/11	
56		Detailed Design Report	11 days?	Sat 11/5/11	Thu 11/17/11	
57	✓	Ovoo meeting - tasks	1 day	Sat 11/5/11	Sat 11/5/11	
58	✓	Work on report	1 day	Fri 11/11/11	Fri 11/11/11	57
59	✓	Ovoo meeting - update	1 day?	Sat 11/12/11	Sat 11/12/11	58
60	✓	Review report - weekly meeting	1 day?	Tue 11/15/11	Tue 11/15/11	

Completed Tasks -ME

8		**MECHANICAL ENGINEERING SIDE**	**87 days?**	**Mon 10/3/11**	**Fri 1/27/12**	
9		**STRUCTURAL SUPPORT**	**87 days?**	**Mon 10/3/11**	**Fri 1/27/12**	
10	✓	Idea Generation Phase	8 days	Mon 10/3/11	Wed 10/12/11	
11	✓	Idea Evaluation	1 day	Tue 10/18/11	Tue 10/18/11	10
12	✓	Feasible Approaches	1 day	Wed 11/9/11	Wed 11/9/11	11
18		**ENCLOSURE DESIGN**	**31 days?**	**Fri 11/4/11**	**Wed 12/14/11**	
19	✓	Get PCB sizes	1 day	Fri 11/4/11	Fri 11/4/11	
20	✓	Get approx cooling system size	1 day	Fri 11/11/11	Fri 11/11/11	19
26		**Cooling Ststem Design**	**61 days?**	**Mon 11/7/11**	**Fri 1/27/12**	
27	✓	Get board Measurments	1 day?	Mon 11/7/11	Mon 11/7/11	
28	✓	Get FPGA chip max running temp	1 day?	Mon 11/7/11	Mon 11/7/11	
29	✓	Design Sstem	2 days?	Mon 11/14/11	Tue 11/15/11	
30	✓	Find best metal for conduction/ material selection	1 day?	Mon 11/14/11	Mon 11/14/11	

Presentaion Dedicated to J. Pascal Desmangles

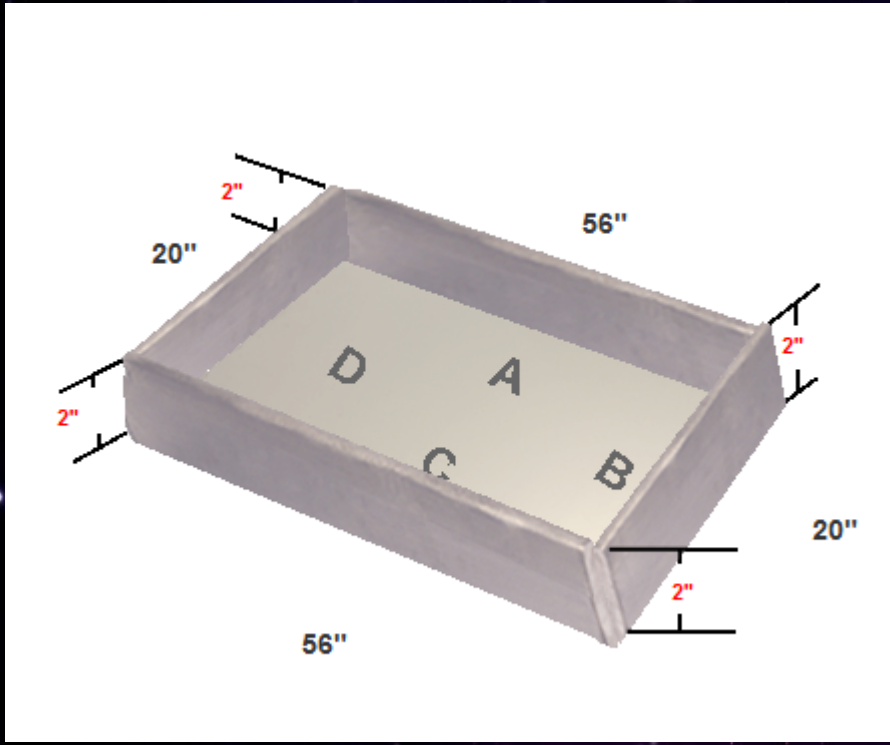
Bright Spirit, Brilliant Mind, Devoted Teammate

Questions?

Works Cited

- Ashby, Michael F. *Strengh vs Density*. Digital image. *Grantadesign.com*. Web. 3 Nov. 2011. <http://www.grantadesign.com/download/charts/new_strength_density.pdf>
- *Cosmicrays2*. Digital image. *Http://www.aspera-eu.org*. Web. 3 Nov. 2011. <http://www.aspera-eu.org/images/stories/Media/MEDIAPICTURES/HR/cosmicrays2.jpg>.
- Cosmic Inquirer blog by Miichael P. Frank.

Appendix



Detector Support Design

Material Selection

- **Need To use plots from Ashby's textbook to find the best material**
  - **Material Index**
    - **Shows which guide lines to use**
    - **Gives an idea of which plots to use**
- **Must use Modulus vs. Relative cost plot**
  - **Relative cost**
    - **Necessary to correct values and remove influence of inflation and units of currency**

$$C_{v,r} = \frac{\frac{Cost_{material\ selection}}{kg} * Density\ of\ material\ selection}{\frac{Cost_{steel}}{kg} * Density\ of\ mild\ steel\ rod}$$

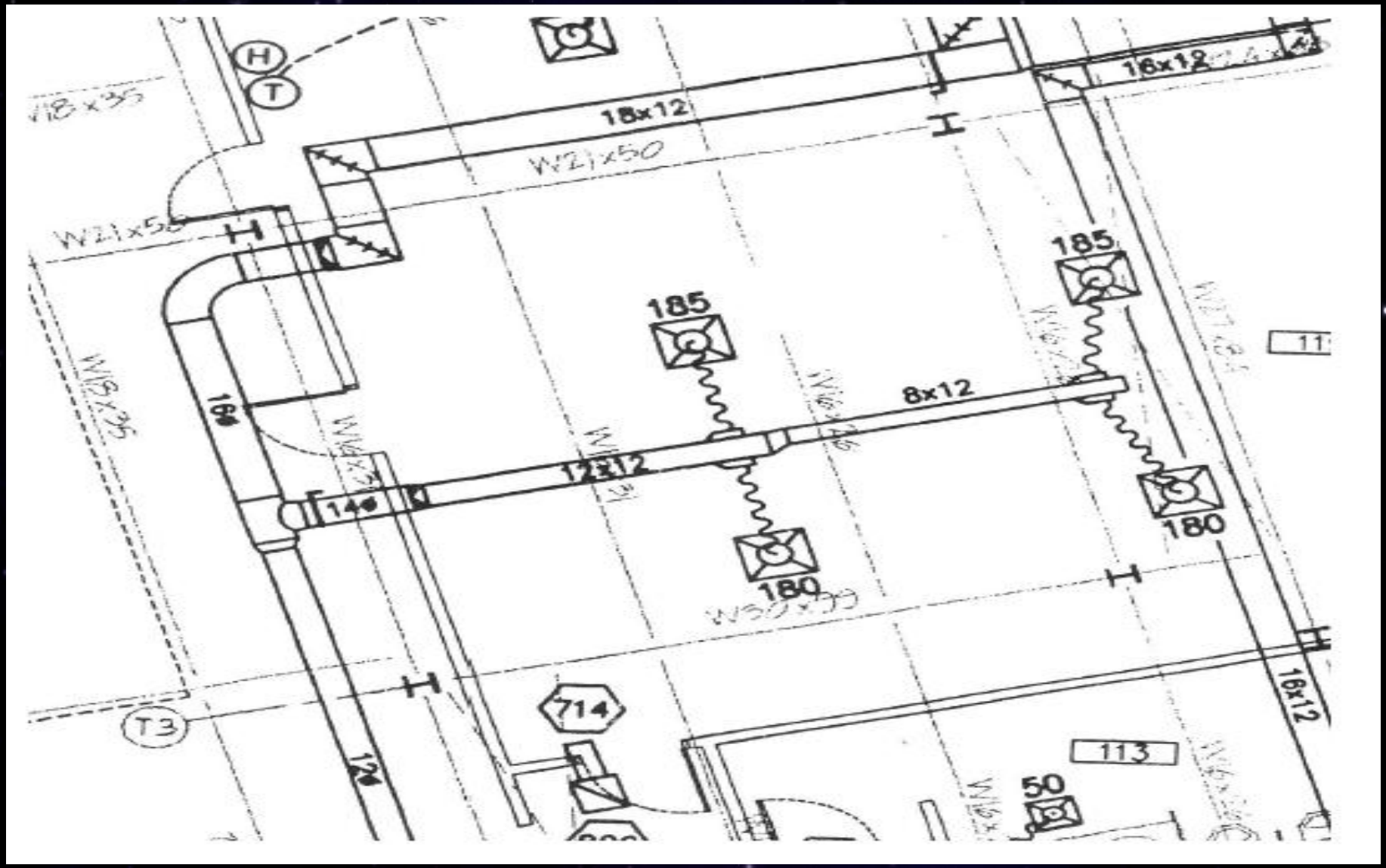
Process selection

- Wood is a natural material
- Birch plywood is prefabricated in sheets with specific thickness and sizes
- The only Real feasible option for processing wood is conventional machining
- The finishing process will involve sanding and coating with varnish to bring out the natural aesthetics of the wood grain

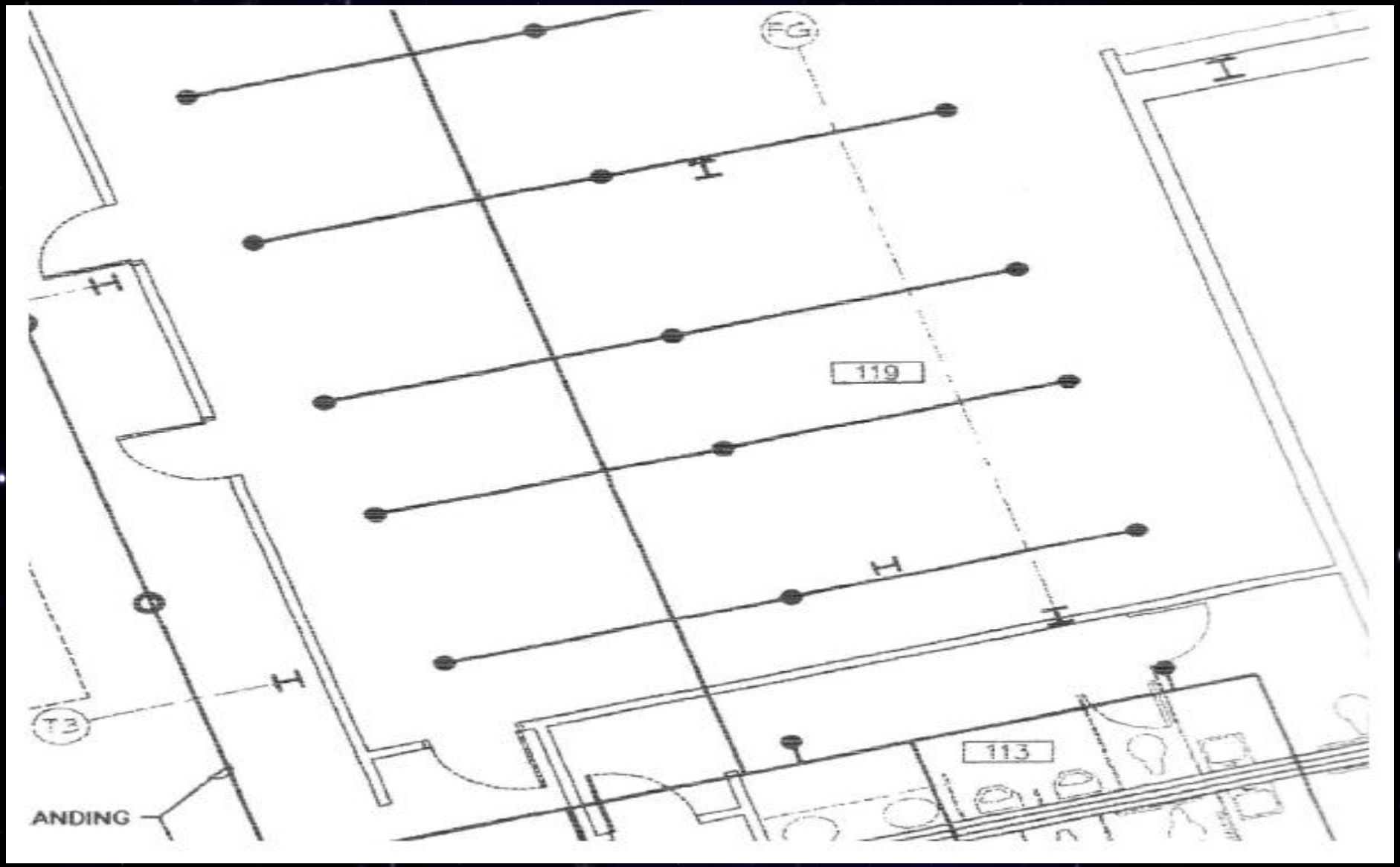
Material Choice: References

- *Aluminum Plate*. Digital image. *Made-in-china.com*. Web. 29 Nov. 2011. <http://image.made-in- china. com/2f0j00bBpEIOzJZvuV/Fireproof-Aluminum- Plate.jpg>.
- Ashby, M. F. *Materials Selection in Mechanical Design*. Burlington, MA: Butterworth- Heinemann, 2011. Print.
- *Baltic Birch Plywood*. Digital image. Web. 29 Nov. 2011. <http: //images.rockler.com/rockler/images/63388-01- 200.jpg>.
- "MDF Board FAQ - Tutorial." *DIY Audio & Video - FAQs, Tutorials, and Calculators for Speaker Boxes, Crossovers, Filters, Wiring and More*. Web. 29 Nov. 2011. <http://www.diyaudioandvideo. com/FAQ/MDF/>.

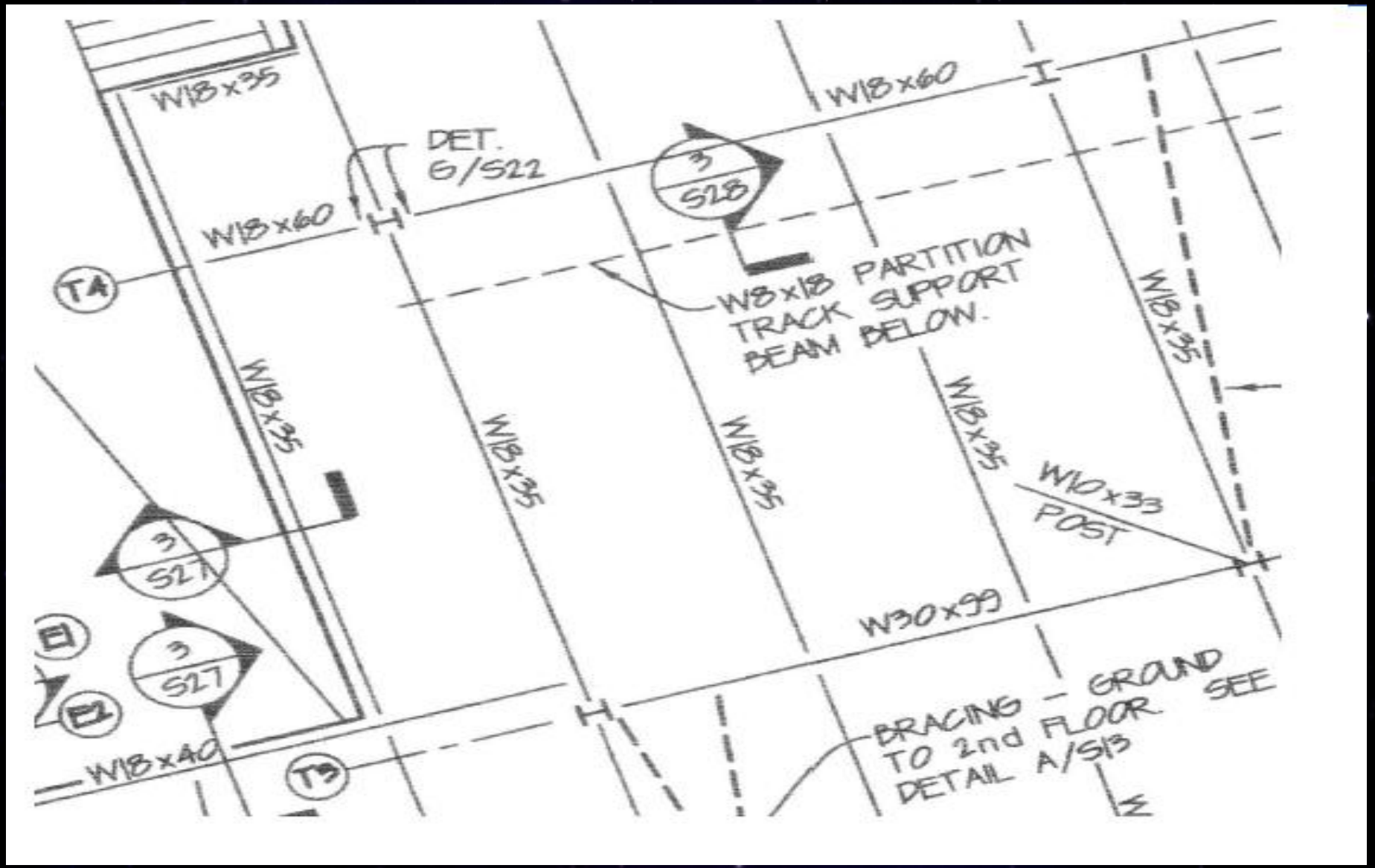
Drawings (vent)



Drawings (sprinkler)



Drawings (iBeam)



Drawings (electrical)