FAMU-FSU College of Engineering
Department of Electrical and Computer Engineering

EEL4911C – ECE Senior Design Project I

CONCEPTUAL DESIGN REVIEW

Project title: **COSMICi**

Team #: 06

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Senior Design Project Instructor: **Dr. Michael Frank**

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November 17, 2011

Executive Summary   (Aarmondas)

The COSMICi Project aims to create a large distributed network of localized, wireless cosmic-ray sensor sub-networks. Many of the sensor networks will be stationed in learning centers such as: the Challenger Learning Center in Tallahassee, Florida high schools, and science museums. These scintillator sensors will detect ultra-high energy particles produced by cosmic ray showers. The light emitted from the high-energy particles from the scintillator will then be amplified using a Photo Multiplier Tube (PMT) and then transmitted to a FPGA board.

The FPGA board will then digitize the voltage pulses from the scintillator detectors and wirelessly transmit this data to a central server (a kiosk). The central server will then log and triangulate the source of the cosmic ray shower events. The information will then be displayed to an end-user.

Eventually the data collected by the scintillator sensors will contribute data to MARIACHI (Mixed Apparatus for Radar Investigation of Cosmic-rays of High Ionization) data sets which will help astrophysicists have more information about the occurrence of cosmic ray showers events.

Table of Contents

Introduction (Pascal)

The COSMICi Project design is approaching conceptual completion. The system's low circuit speed is being addressed on both the software side and the hardware side. The software team is working on reducing component blocks and firmware code while the cooling system team is tailoring a Peltier cooler to the needs of the system based on measured data. A power source has been devised and the central server configuration is nearly complete. Various materials are being evaluated for the circuit boards enclosure. The structural support has been finalized and parts will be ordered soon.

Acknowledgements (Pascal)

Acknowledge outside contributors, advisors, etc.

Problem Statement (Pascal)

Problem Statement

The objective of this project is to install a fully functional cosmic ray "telescope" at the Challenger Learning Center in downtown Tallahassee, Florida. The system will be installed according to a configuration that allows it to triangulate the origin of a cosmic ray shower and display the results on a computer screen.

General Solution Approach

Fully Functional

The engineering team will have to address a few system "inner workings" issues before installation.The team will have to solve the following: slow processing speed, maximum number of detectors that can be handled by the processor,data display, cooling system, protective enclosure, and structural support.

Configuration

The detectors will ideally be placed 30ft apart in a triangular configuration and communicate via data cables to a main processing unit which will wirelessly send the display information to a kiosk.

In an upgrade configuration (Stage 2), each detector will have its processing unit and wirelessly send the display info to the kiosk. This configuration will require the design of a synchronizer that will ensure that the detectors have the same time reference.

Operating Environment (Aarmondas)

These devices will be implemented in learning zones (such as the Challenger Learning Center – Tallahassee, Florida), schools and other academic learning facilities. As such, they will need to have durable cases that can prevent any damage to the components should students or visitors throw objects at the system, or try to touch the systems. The casings should also prevent the system from negatively impacting the environment around it. Since the devices are not required

to be in a well lit environment, they can be kept somewhere that the sun and other weather elements would not directly affect them. Also the devices should not be placed in direct sunlight as direct sunlight may result in unwanted particle detection.

Intended Use(s) and Intended User(s) *(Aarmondas)*

The Challenger Learning Center has agreed to have the COSMICi project implemented in their facility. This design project will enable the user to triangulate the point of origin of cosmic rays that enter earth's atmosphere. Cosmic rays can originate from exploding stars, the suns magnetic field, and a number of other cosmic events. The study of the origin of these cosmic rays is vital to understanding matter outside of this solar system. It can provide a genetic blueprint of the chemical composition of the universe.

In implanting this project in the Challenger Learning Center, this project also serves as a learning experience to the new ambitious young minds of this generation. Along with helping researchers continue to map the chemical composition of matter far outside this planet's atmosphere.

This device will benefit astrophysicists in mapping and collecting data on different events occurring in the universe, such as merging black holes, star deaths, and other high energy occurrences. These systems will be portable enough for individuals to set up and gather data to contribute to the global data server, as well as being set up in learning centers, schools and other locations to increase the amount of global coverage and collection of data.

Assumptions and Limitations *(Mike)*

After solidifying the groups overall project goals the following assumptions have been created:
- The system will consist of at least 3 sensors in order to triangulate the direction of the detected high-energy particles
- The sensors will share a GPS input to time-stamp the data at its initial detection time
- The Electronic components (FPGA Board, Power System, Cooling System, GPS Module, WIFI board and Central Timing Unit) will be contained in an enclosure for safety
- A cooling system will be needed to reduce the temperature of the FPGA board to an ideal temperature of 2° C
- The sensors and circuit board enclosure will need to be mounted with the sensors forming an equilateral triangle with 30 feet of space between any sensors
- The FPGA's high-speed components will need to operate at a frequency of 500MHz (those using the PLL (Phase-Locked Loop)
- Reductions in memory will be made to allow for the incorporation of additional sensor inputs (at least one) and a synchronizing timing input
- The system will be able to keep an internal count of the time the data comes in relative to the current 56-bit width counter in the FEDM coding (CALCULATE TOTAL TIME)
- A battery source using 2 NiMH batteries and a power supply (recently discovered in a usable location) will be powering components for the project

The following are the limitations for the group to adhere to:

- The FPGA board must have a functional frequency of 500MHz to ensure the desired ±1 ns between data readings
- The FPGA's chip must be cooled to about 2 ºC ± 2ºC and the overall board should be about 25 °C ±5ºC (this will help the FPGA to operate at 500MHz without overheating)
- The amount of code that can be reduced will be limited by the necessary features of the project to operate correctly
- Most of the standard libraries must be kept due to their heavy influence in keeping the firmware fully operational
- The FPGA board for the FEDM has a limited amount of memory locations compared to what needs to be implemented on the board (this may require more optimizing of used memory to fit in more inputs)
- The mounting cannot be implemented until the enclosures are completed
- The mountings, if hung below the ceiling, must be high enough so that they are not a hanging hazard for pedestrians
- The support structures need a spacing of 30 feet and must not interfere with any water sprinklers, air conditioners or any other unsound structural supports
- All cables must be enclosed in a conduit so that there are no electrical hazards with open cables
- There is little funding for materials to enclose the FPGA board, so scrap metal from the mechanical labs may be utilized (since this is partly a prototype enclosure there are no specific material requirements as long as the design is safe and protects the devices)

Expected End Product and Other Deliverables (Juan)

Weekly reports??
Incorporate Dates.

- Phase I:
  - COSMICi System will detect UHECR from at least 3 scintillator devices
  - The direction and source of the cosmic ray shower will be displayed to the user in the kiosk computer in the form of a sky map (possibly physics dept. task).
  - A power source will be configured to supply all the components
  - An enclosure will protect the circuit boards
  - A Cooling System will maintain the FPGA chip at 0 C
  - A structural design will support the scintillator-detectors and the enclosure

- Phase II (if time permits)
  - When the project enters into Phase II there will be one FPGA board for each detector and a wireless optical synchronization clock system
  - Mirrors will be installed to direct the synchronization pulse to the receivers in each FPGA.
  - Optical Timing Synchronization will be incorporated into the detector system
  - A new PCB design of the current board will be created, fixing bugs and errors on

This component should list, along with a brief description, the end product and any other items that will be delivered to the client from this time through to the end of the project. If the end product is to be commercialized, the description shall be of the commercialized end product. It shall be in the form of a technical product announcement, as opposed to a product advertisement, and **shall not include a list of technical specifications. Delivery dates shall also be specified.**

System Design

This section is where you lay out the current state of the overall design of the system you are developing.

Overview of the System (TBA @ next Meeting week of the 14th)

Description, block diagrams, drawing and pictures (as appropriate).

Major Components of the System, (individual)

Brief descriptions of all the major components of the system.
Detectors
(George will take care of this with the science behind it?)
        The main components of the system are the four scintillators that will be placed on the support structure. Scintillators detect and absorb the incoming radiation through Earths atmosphere created by solar rays, supernovas, dark matter, and other uncertain origins from beyond this atmosphere. In particular, the detectors absorb the sub atomic particles called muons, which are created from the decay of pions and kaons. With the implementation of the network system, these detectors will be able to help triangulate the point of origin from incoming cosmic rays.

Front-End Digitizer Module (Stratix II ----> $50K)

        The Front-End Digitizer Module takes the analog signals coming from the scintillators and digitalizes them … (EXPAND ON THIS!!!)

FEDM Control Software
        The FEDM Control Software is being prototyped on an Altera DE3 development kit and is using a Stratix III FPGA. ?
FPGA Stratix II (FEDM) - 50K Custom Board - Connected to the PMT (converts the Analog to Digital)
FPGA Stratix III - DE3 Board Control Software(the middle man that gives the commands)

Wi-Fi Module and Development Kit
        Current Wi-Fi board is a Laird EZURiO WISMC01BI /WISDK01BI-02. This is used to establish a data connection between the FEDM and the Central PC Kiosk.

GPS Sub-System
        This consists of a GPS module that sends a serial input stream and a timing sync reference signal to the DE3 board. This acts at a absolute reference to "real world" time, rather than a relative clock cycle value. A 10MHz signal is sent from the high precision oscillator (timing reference board) which acts as a relative signal that starts when the board begins running.

Structural Supports
The structural support system consists of the following for each detector: 4 i-beam clamps, 4 threaded rods, and a wooden platform . Each of the threaded rods will have one of their end be bolted to a corner of the platform. The other end will be bolted to a clamp which will be fastened to a side of the i-beam.

Enclosure
The enclosure will consist of an aluminum housing with a plexi-glass door. The structure will contain all the circuit boards, the power supply and the cooling system.

Cooling System
(George will take care of this)
      The cooling system consists of copper tubing, a peltier cooler, copper heat sink fins, and a fan to remove heat from the system. Heat generated by the FEDM chip will travel through the copper piping to the peltier cooler which will create the heat dispersal through the fins and fan.

Power
      All components are currently being powered by outlets and an adjustable power source in the lab. Since the goal is to have these implemented in the Challenger Learning Center, we need an alternative solution for powering every component.
There is a suitable power supply in the lab that we will use to provide power for the FEDM, CTU, and two of the Detectors. The third detector will be battery powered.

Performance Assessment *(individual)*

Assessment of how the system will meet the needs and requirements for the project (refer to the Needs Analysis and Requirements Specifications report you have already submitted).

Structural Support
      The support system will allow the detectors and the circuit board enclosure to be safely suspended from the ceiling in accordance to the safety rules enforced at the Challenger Learning Center. The center's safety representative requested that all hanging equipment be attached to the building structure i.e. I-beams. The structural support design meets the requested safety guidelines and also load requirements with a high safety factor . Each scintillator weighs 25 lbs and the corresponding set of beam clamps supporting the detector has a combined capacity of 2000 lbs(4 X 500lbs).

Power Supply
Each component of the project has to be supplied by a certain amount of power. Power for the CTU, the FEDM, and two of the detectors will be provided by a 250W power supply. This power supply holds voltages of 12V, -12V, 5V, 3.3V, and a GND (0V). All voltages for each component of the project can be supported. The total power is well under 250W so this power supply holds more than enough power to provide to each component.
The third detector will be battery powered by a 12V, 5Ah NiMH rechargeable battery. This

detector will be used for demonstration purposes. The detector requires a current of 21mA with 12V so this battery is definitely suitable to provide power for a long period of time before needing to be charged.

Enclosure

The enclosure will house all the PCB's and power supply. It will protect them from physical shock and foreign object debris. The enclosure will be hung from the ceiling with a clear cover so that all components are easily viewable for the public. The enclosure will have vents to support the airflow throughout the system. The enclosure will house the cooling system and be supported by a structural support. The clear cover will be hinged and keyed for secured access to the boards and power supplies in order to make changes.

Cooling System

The cooling system design will provide greater than three times the heat removal from the FEDM chip. Using copper instead of the current aluminum block, the heat transfer rate increases from 120 W/m*K to 401 W/m*K. Also using copper heat fins, the fan will dissipate the heat from the system at higher rate as well.

Bit-Width Reduction

In order to add an additional sensor input and time-stamping input from the GPS, the FPGA board will have to free up some memory. To free up this memory the bit width size used in the FIFO and Pulse-Path components was reduced from 64 bits to 56. This freed up the space needed for additional inputs. There is now enough room to add the additional sensor input data path, and begin implementing the GPS timing input path to time-stamp the data.
The results of the freed space are as follows:

Before:
- Slow corner fmax for high-speed counter: 211.28 MHz
- Logic utilization: 24,314/27,104 (90%) = 2,790 remaining
- Dedicated logic registers used: 21,878/27,104 (81%) = 5,226 remaining
- M512 blocks: 193/202 (96%) = 9 remaining
- M4K blocks: 144/144 (100%) = 0 remaining
- M-RAM blocks: 1/1 (100%) = 0 remaining (but we may be able to use a bit more of the space)

After:
- Slow corner fmax for high-speed counter: 213.13 MHz (only slightly better)
- Logic utilization: 22,007/27,104 (81%) = 5,097 remaining (almost 2x as much left)
- Dedicated logic registers used: 19,463/27,104 (67%) = 7,641 remaining (about 25% better)
- M512 blocks: 188/202 (93%) = 24 remaining (more than 2x better)
- M4K blocks: 144/144 (100%) = 0 remaining (same as before)
- M-RAM blocks: 1/1 (100%) = 0 remaining (same as before)

-From Dr. Frank's blog at http://cosmicinquirer.blogspot.com/

FPGA Operational Frequency Increase

All high-speed components of the Front-End Digitizer Module (FEDM) will be logically optimized using Quartus' Logic Locking feature. This will be utilized to bring the FPGA board back from its current 200MHz operational frequency to the prior 500MHz. Using logic lock will prevent Quartus from "optimizing" the logic elements in the way it sees fit and keep the designers exact specifications in order to reduce the amount of memory usage. All of the circuit components that use the Pulse-Locked Loop will have to be logic locked. This is also a part of the projects goal to free up memory on the board for additional inputs.

Front-End Digitizer Module (Firmware)

Design Process (individual)

Review of major design decisions that have been made (or remain to be made).

Structural Support

The current structural design may need to be modified. It has not been decided yet on whether the equipment will hang below the drop ceiling or be above it. Further more, the client expressed the desire for detectors to be spread across the 2 adjacent classrooms @ the CLC. A team member will met with Dr Frank and O'Neal on Nov 15th. It was recommended that the support system did not block or interfere with any sprinklers or air ducts. Also one of the scintillator-detector supports will be slightly modified to accommodate two batteries that will power the detector.

Enclosure

The enclosure design is finalized all components fit perfectly with some room.

Power Supply

A breadboard solution is the best decision for powering the CTU, FEDM, and the two detectors. A clean connection of jumper wires from the power supply and the other components will be connected to a breadboard.
For the battery powered detector, we will use two of the NiMH rechargeable batteries and connect them in parallel. We will need a connector for the batteries and a barrel plug to insert into the detector.

Bit-Width Reduction

To effectively reduce the bit width size generic values were implemented in the h_speed_counter, fifo_reader, fifo_writer, cs_combine, se_pulse-cap and stream_pulse_data so that future size changes to the bit width will be simple to implement. Once the code for the VHDL and Verilog components was edited they were recompiled and renamed with _56 tags. Next the code was recreated into blocks diagram from the lowest level, where they were then recreated up to the top-level of the block diagrams. Once this was completed it was given to Dr. Frank to implement into the current top level diagram. After some debugging the code was added to the project and freed up more memory and allowed for the next steps of implementing

additional inputs.

FPGA Operational Frequency Increase

All high-speed components of the Front-End Digitizer Module (FEDM) will be logically optimized using Quartus' Logic Locking feature. This will be utilized to bring the FPGA board back from its current 200MHz operational frequency to the prior 500MHz. Using logic lock will prevent Quartus from "optimizing" the logic elements in the way it sees fit and keep the designers exact specifications in order to reduce the amount of memory usage. All of the circuit components that use the Pulse-Locked Loop will have to be logic locked. This is also a part of the projects goal to free up memory on the board for additional inputs.

Design of Major Components *(individual)*

This section is designed to give more details on the status of the major components of the systems being designed. This is one of the major sections of the report.

The format for this section of the report should be approximately as follows. It should begin with a brief statement and then have the following have a subsection for each of the blocks in Section 2 System Design:

<title of block 1>

These subsections shall include a description of the block/component including a description of the decision process and analysis conducted leading up to the current design (requirements, design parameters, <u>alternatives considered</u>, etc.). Also include block diagrams, drawings, photographs, circuit schematics, flow charts, pseudo code, etc. as appropriate for the block or component. <u>If there is a specific risk associated with this block, identify and describe the risk and refer the reader to the appropriate section of the risk assessment given in Section 6.</u>

The goal is to demonstrate the status of the block, the design process used, the ability of the block to meet the requirements (assessment of design), and the current risks associated with this component. You subsections as needed to discuss the sub-blocks of this major block.

Any needed data sheets you think are important should be included in an appendix to the report.

<title of block 2>

8. ## Power

- ### FEDM, CTU, Two Detectors

    The power for the FEDM, CTU, and two Detectors will be provided by a 250W power supply. This supply has several voltage levels that will be connected to a breadboard. To share certain voltages, components of the project must be connected in the same node as the voltages from the power supply. The FEDM jumper wire will be connected in the same node as the 5V voltage level from the power supply; along with the CTU and GPS evaluation kit. The 12V voltage level from the power supply will be connected in the same node as the wires from the two detectors. These wires will be soldered to two barrel plugs and then inserted into the detectors. Since other components of the CTU require 3.3V, there will be an additional connection for the DE3 board. It would share the same node as the 3.3V voltage level from the power supply.

- ### Detector
    The third detector will be used as a demonstration and would be battery powered as a request from Dr. O'Neal. The detector requires 12V at 21mA. The battery that will power this detector will be a NiMH 12V, 5Ah battery. Having two of these batteries connected in parallel will result in a 12V, 10Ah battery. A battery

with these values would last approximately 3 weeks (based on the measured values of the detector). To make this connection we will need a connector to connect both positive sides of the battery together. In addition, a connector to connect both of the negative sides together is also needed. We will then need extra connectors that can be soldered to a barrel plug. When this connection is complete, the barrel plug will be placed into the detector to provide the power.

Bit-Size Reduction

In order to free up space on the Stratix III board for additional inputs the current bit-width of the "relative time" clock cycle timing counter. This consisted of reducing the bit width of several components from 64 bits to 56 bits wide. Once the coding was reduced the block diagrams had to be relabeled as well. After the block diagrams we relabeled the new block diagrams, VHDL code files and Verilog code files were incorporated into the main design file and tested for errors.

Images of reduced block diagrams before and after (just a few for example purposes not all of them)
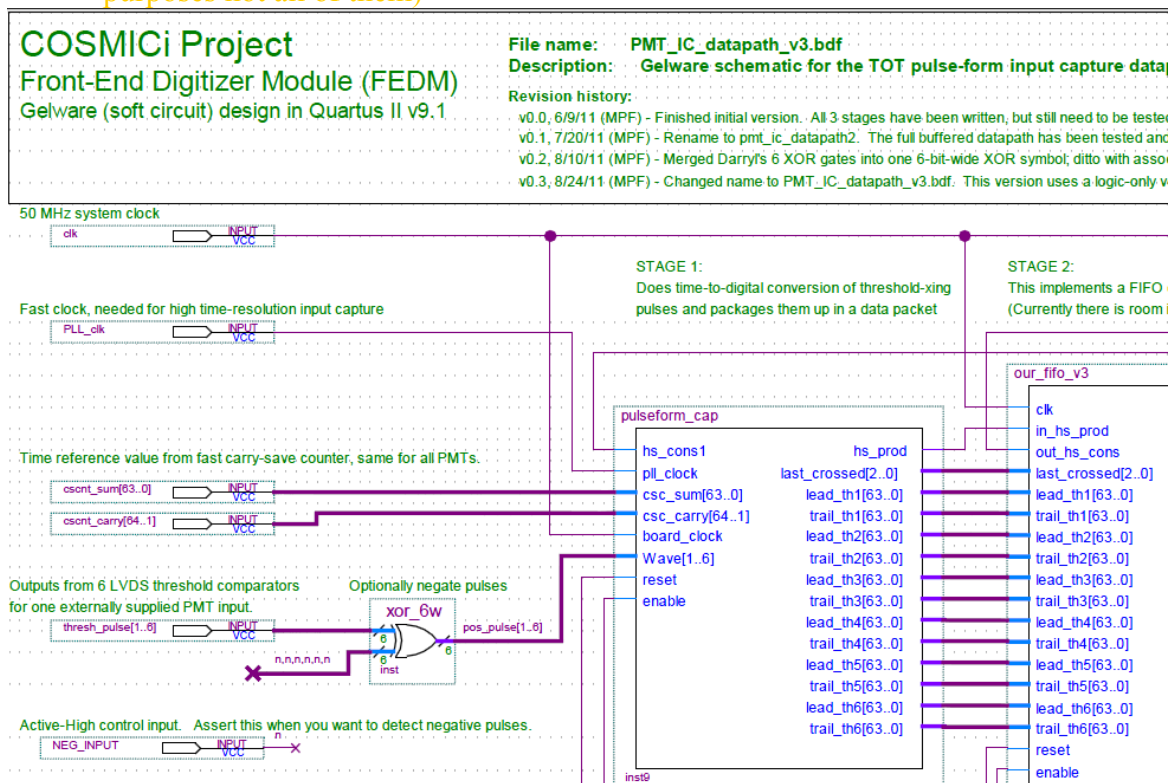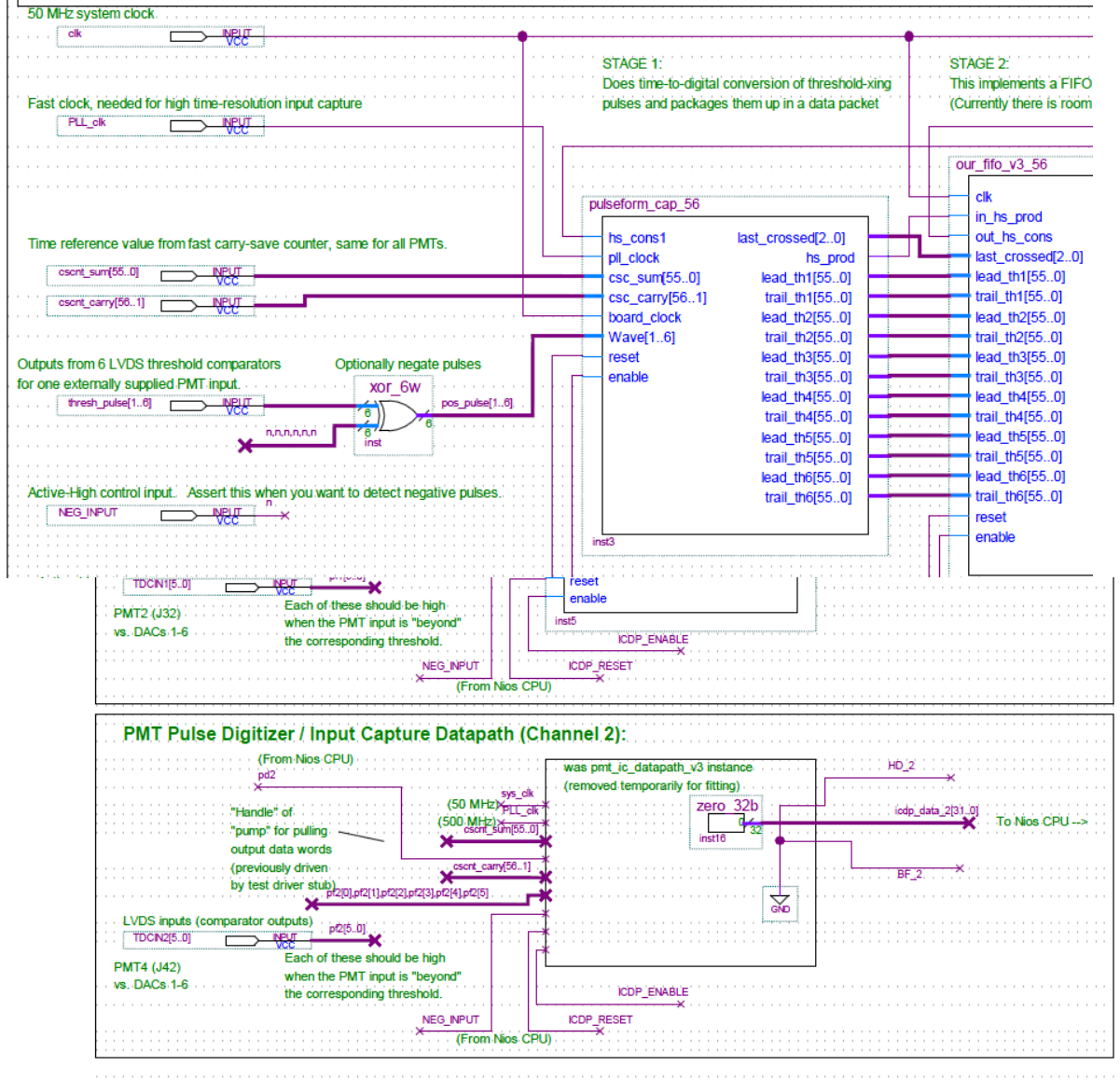

Above is an image of the block diagram before the bit reduction
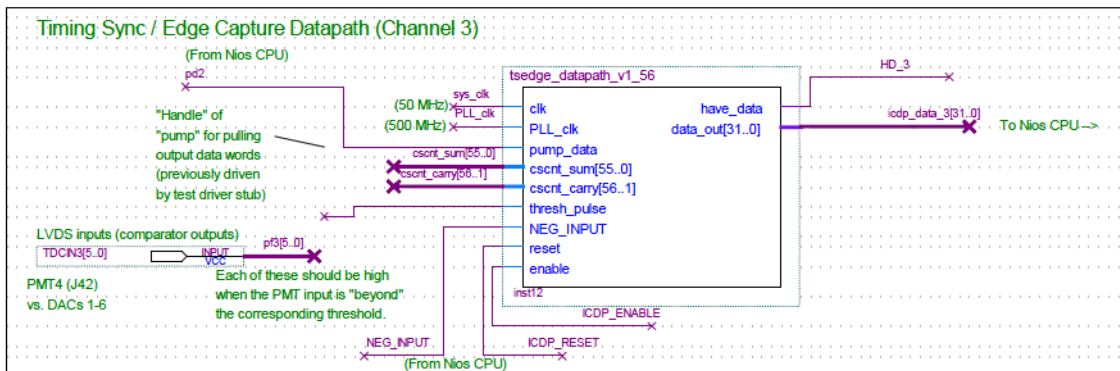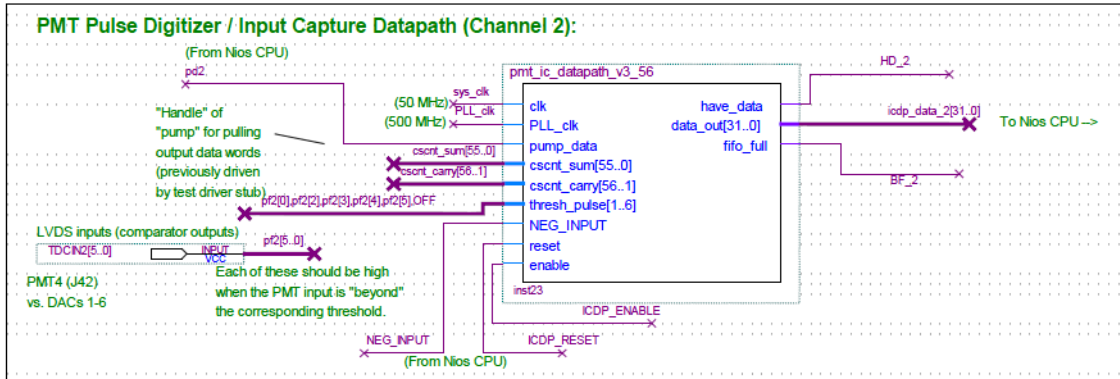Below is an image of the same block diagram after the bit reduction

Above is an image of the Top level diagram before the third input could be incorporated
Below is the image with the third input added to the design

PMT Pulse Digitizer / Input Capture Datapath (Channel 2)

Timing Sync / Edge Capture Datapath (Channel 3)

9. ## *Logic Lock High Speed Components*

This section of the project will consist of speeding up the FPGA's operational frequency to its initial 500MHz. Currently it is operating at about 211MHz and does not give the required margin of 2 ns between each data reading.

The Quartus logic locking feature will be utilized to ensure that the components operate at 500MHz and that Quartus won't add additional logic elements that might slow down the clock.

Structural Support

1. *Early Designs*
   Wall Support Design
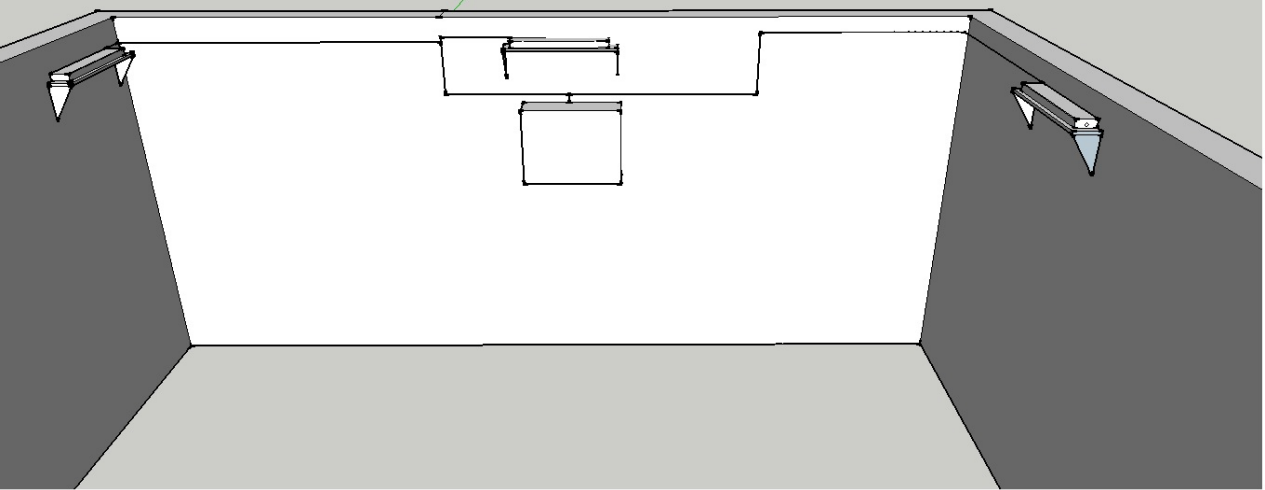
1.
Description
- In this configuration, the COSMICi elements are supported by structures attached to the walls. Each element will be carried by a shelf. The shelf will be supported by a heavy duty bracket.

2.   Reasons for rejection
- The classroom walls are made of Sheetrock.
- Challenger learning Center Safety guidelines mandate that all hanging components be attached to I-beams.

Ceiling Support Design
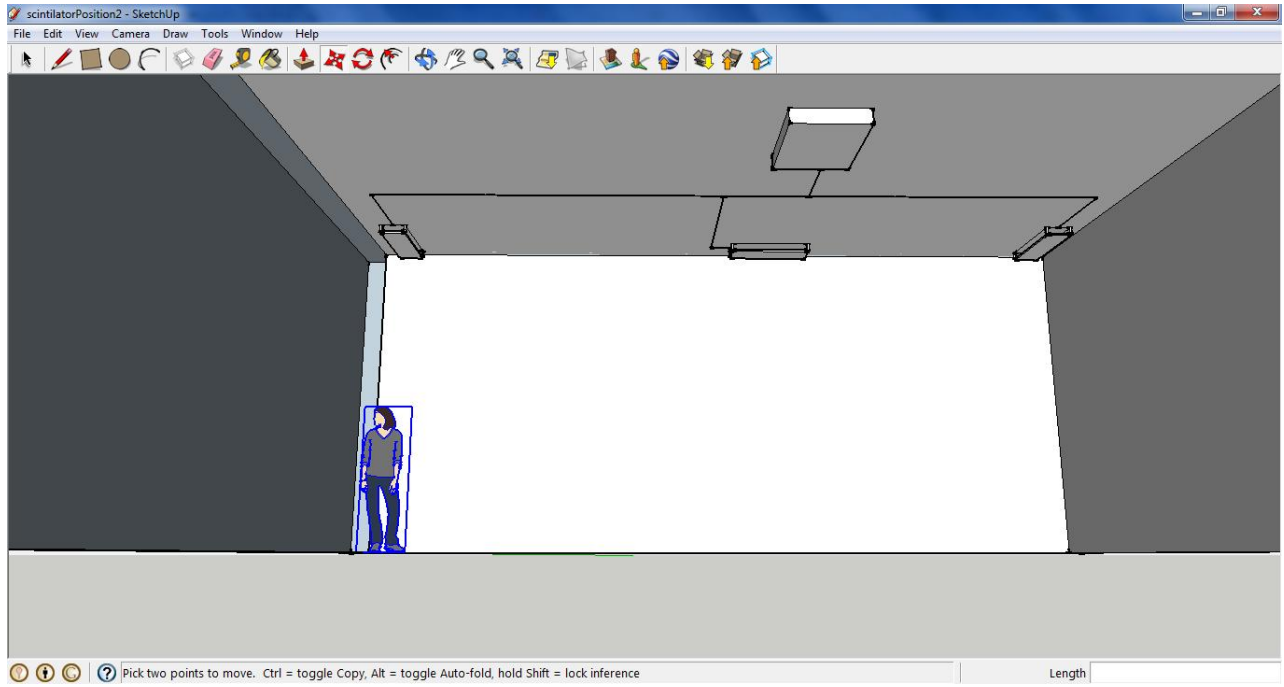
1. Description
   - This arrangement puts the COSMICi components a few inches below the ceiling. Each element will be supported by a platform. The platform will hang from the ceiling through a combination of brackets, bolts and anchors. Four holes will drilled in the ceiling and anchors will be wedged in them. The static friction between the anchors and the ceiling material will provide the required force to support the component's weight.
2. Reasons for rejection
   - The classroom's ceiling is not made of concrete
   - Challenger learning Center Safety guidelines mandate that all hanging components be attached to I-beams.

3. *Actual design*
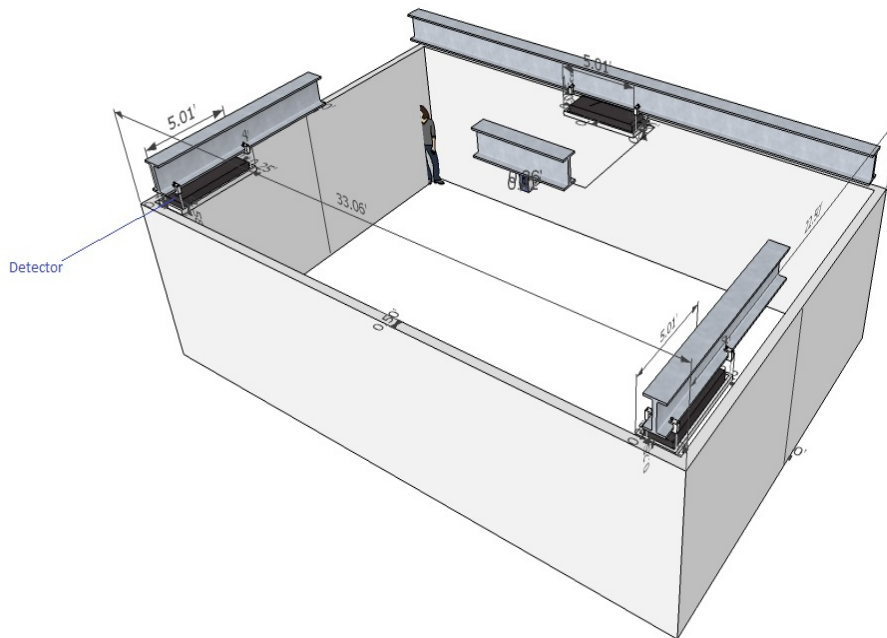
The current design consists of 3 scintillator-detectors forming a triangular configuration and a circuit board enclosure. They will all be hanging from I-beams in room 119 at the Challenger Learning Center. Each side of the triangle must be 30ft long with a tolerance of 2 to 3 ft. One of the detector support platforms will also support two 2.2 lbs batteries.
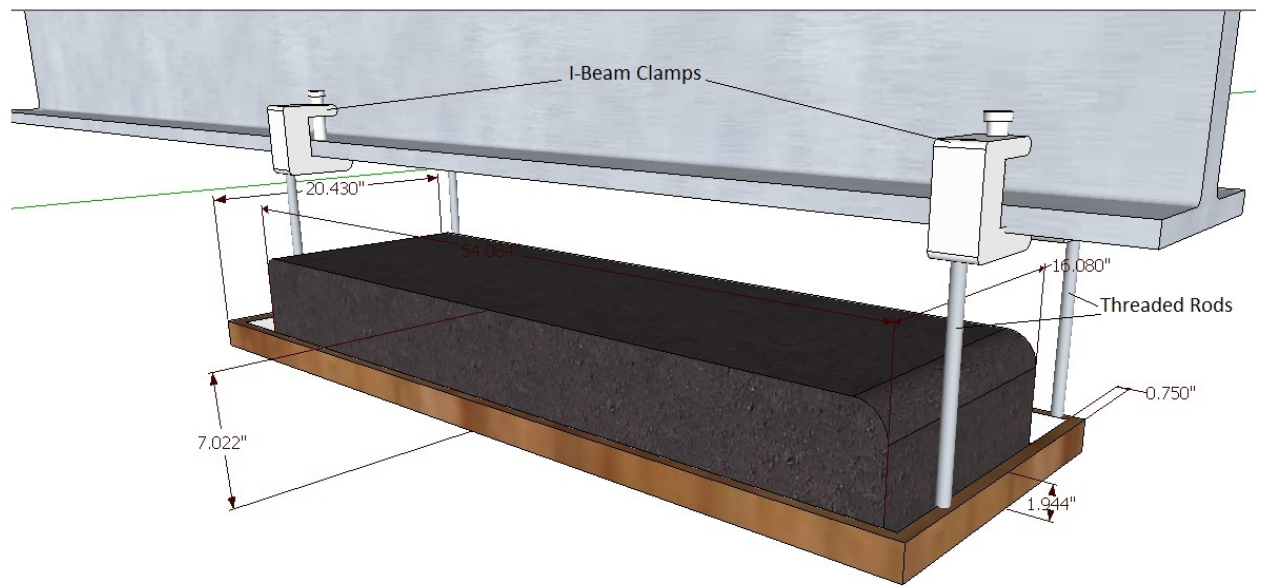
ENCLOSURE;

The clear cover is most likely going to be made of acrylic plastic, while the base will be made from plate aluminum. The cover will be attached to the baseplate by a sevral hinges on one side and a keyed lock on the other for easy, yet secure, entry and access to the enclosed components.
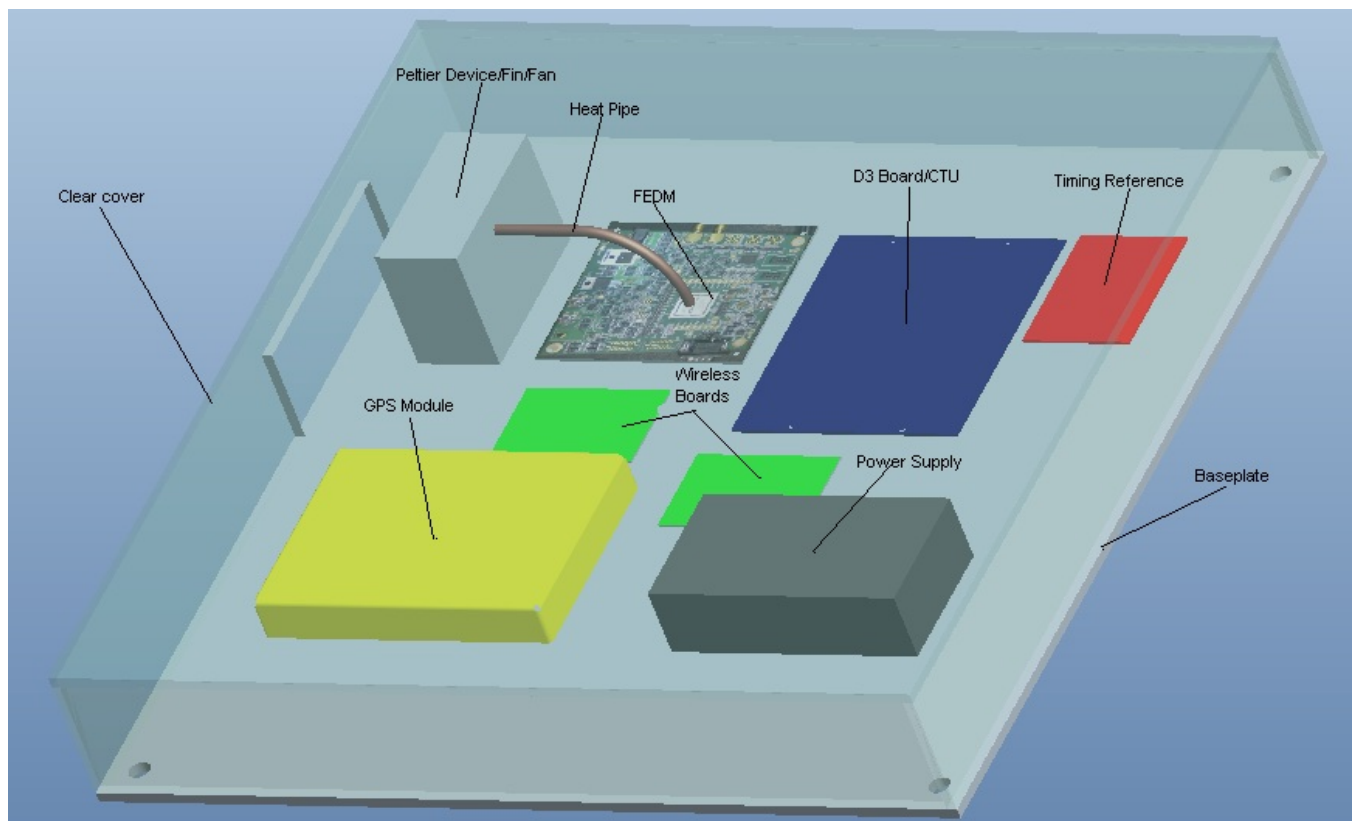
Cooling System

       The final designed cooling system will include the initial and current implemented system along with added materials to decrease the temperature of the chip and the surrounding voltage regulators. The aluminum block will be replaced with a solid block of copper due to its higher thermal conductivity of 401 W/m*K compared to Aluminum's 120 W/m*K. With the mounted peltier cooler attached to the heat removal fan and new copper heat sink fins as the current system is set up, the higher heat transfer rate will remove more heat produced from the chip creating a lower operating temperature from the current 8oC.

       Although using copper will increase the heat rate transfer from the FPGA chip, it will still create condensation build up on the copper block as it does on the current aluminum block. To solve this problem the block will be coated with a spray foam polyurethane insulation. This will eliminate condensation forming on the block and chip and solve the current issue of possible water damage to the chip and board.

The schedule you presented in the Project Proposal should be repeated here. Indicate on the Gannt chart the actual status of the tasks and milestones of the project (for example, use different color to indicate complete). DO NOT modify the schedule to make it look like you all tasks are on time. Summarize how you intend to address schedule slippage or capitalize on early completion of tasks.

Milestones:
1. October 16, 2007: Start Project
2. November 5, 2007: Acquire Microcontroller
   …
A. February 2, 2008: Complete Initial System Integration
   …
B. March 20, 2008: COE Hardware Competition

Percentage Completion

1. Power Supply and Batteries

Power Supply – 80% of Overall Task Goal

Subtasks

- Power FEDM – 10%   DONE

- Power CTU – 10%   DONE

   - Power both CTU and FEDM – 70%

   - Provide Power for detectors – 10%

20 % OF POWER SUPPLY GOAL IS COMPLETE

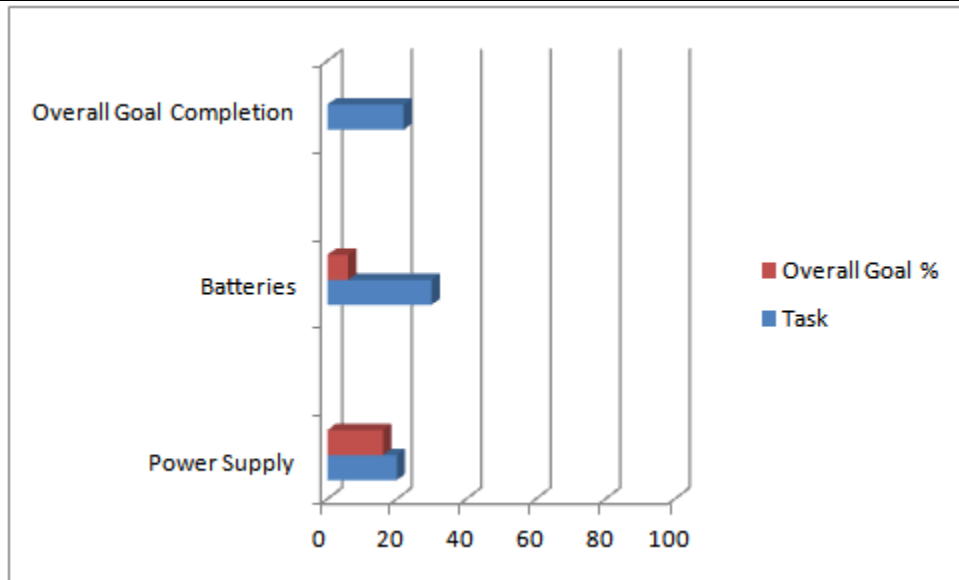Battery – 20% of Overall Task Goal

Subtasks

-      Research – 30 %   DONE

       -      Order Parts – 10%

       -      Implement – 40%

       -      Test – 40%

30 % OF BATTERY GOAL IS COMPLETE

POWER SUPPLY AND BATTERIES PERCENTAGE OF COMPLETION

22% of overall project goal is complete

2. Cooling System

Subtasks

Temperature Measurements of Chip and Board –5%   COMPLETE
Physical Measurements of all Boards – 5%   COMPLETE
Peltier cooler, fins, and fan cad design – 35%   HALF WAY COMPLETE
Provide heat equations showing chip temp – 30%   INCOMPLETE
Design Water Outlet –10%   HALF WAY COMPLETE
Order correct size peltier cooler, fins and fan –5%   INCOMPLETE
Connect cooling system to structure–5%   INCOMPLETE
Test–5%

COOLING SYSTEM PERCENTAGE OF COMPLETION
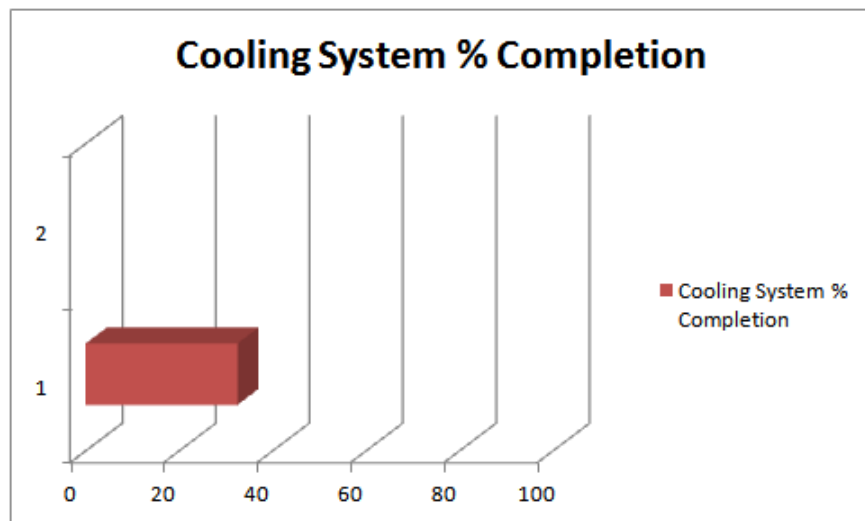
32.5 % Cooling System GOAL IS COMPLETE

3. Freeing Up Memory for Additional Inputs

Current Completion Status: 100%

Subtasks

1) Bit-Width Reduction – **80%** of Overall Task Goal

-	Familiarize with Code – 5%	DONE 9/21/11
-	Implement Global Variables–30%	DONE 10/5/11
-	Recreate Newly Sized Component Blocks – 30%	DONE 10/19/11
-	Re-wire and Re-label Components – 10%	DONE 10/23/11
-	Debug and Test for Completion – 5%	DONE 11/2/11

100 % OF CODE REDUCTION GOAL IS COMPLETE

2) Add Additional Input – 20% of Overall Task Goal

-	Add additional Input VHDL Code – 10 %	DONE 11/2/11
-	Test For Errors – 10%	DONE 11/2/11

100 % OF ADDITIONAL INPUT IS COMPLETE
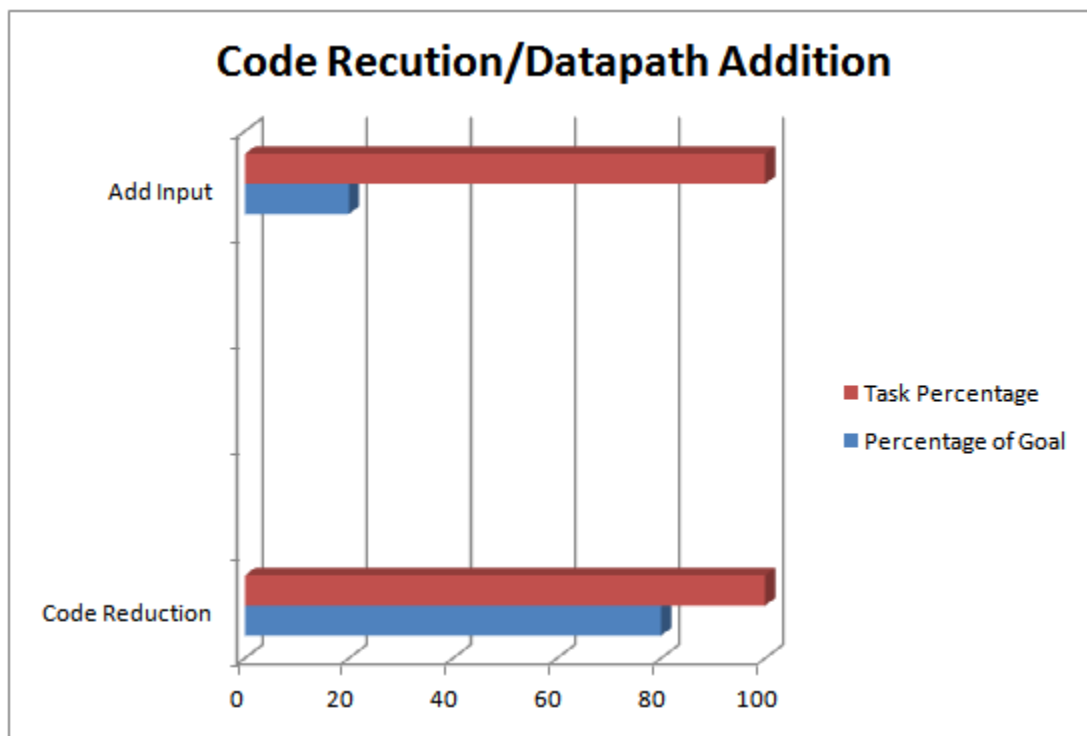
100 % of goal is complete

Timing Sync Data Path (firmware) (20% done?)
- Research system level design (11/5 - 11/18) ----- 30% done
- Implement design (11/21 - 12/9)
- Testing (12/9 - 1/12)

Python Server Visualization (0% done?)
- Research Google Earth API (1/9 - 1/20)
- Implement design (1/23 - 2/10)
- Testing (2/10 - 2/19)

4. Logic Locking High Frequency Components

This portion of the goal has not been started as of yet. The following subtasks need to be completed:

- Research Logic Locking – 5%	TBD	1/9/12
- Logic Lock Lowest Level Components – 25%	TBD	1/16/12
- Test Frequency Operation Level – 10%	TBD	1/23/12
- Logic Lock Additional Levels – 25%	TBD	1/26/12
- Test Frequency Operation Level – 10%	TBD	1/31/12

Testing the clock's operational frequency is a another goal that has not been started yet. The following subtasks need to be completed:

- Test Integration of New Frequency – 15%	TBD	2/8/12
- Test For Errors – 10%	TBD	2/15/11

5. Enclosure

Subtasks:

- Baseplate: 45%
  - Designing : 31.5%
  - Machining: 13.5%
- Clear Cover: 45%
  - Designing: 27%
  - Machining: 9%
  - Fabrication: 9%
- Assembly: 10 %
  - Fabrication: 10%

Overall Project goal completion is 20%

6. Structural Supports

Scintillator Support – 75% of Overall Task Goal

Subtasks

- Scintillator Measurement – 10%   DONE
- Room Measurement– 10%   DONE
- Fastening Method Analysis – 50%   DONE
- Part Ordering-20%
- Design Implementation – 10%

70 % OF Scintillator Support GOAL IS COMPLETE

Enclosure Support – 25% of Overall Task Goal

Subtasks

- Enclosure Measurement – 10%
- Room Measurement– 10%   DONE
- Fastening Method Analysis – 50%   DONE
- Part Ordering-20%
- Design Implementation – 10%

60 % OF ENCLOSURE GOAL IS COMPLETE

Budget Estimate (Brian needs info by Sunday 13th)

Provide an updated budget for the project. It should show the original (proposed) budget and an updated budget based on costs thus far in the project and updated estimates.

As far as the budget goes for the computer programming part, all the licenses, boards, computers and what not are supplied to us, and the licenses were donated to the FAMU lab group so there is no expenditure for those. (Michael Dean)
HOWEVER YOU MAY WANT TO INCLUDE IN THE BUDGET THAT IT WAS COVERED JUST TO SHOW THAT WE ARE ACCOUNT FOR EVERYTHING??

D. Expense	Quantity	Unit Price	
Travel	100.00	$3.50	$350.00
Equipment			
Structural support			
Beam Clamp 3/8"	16.00	$2.39	$38.24
Threaded Rod 3/8"	16.00	$8.89	$142.24
Hex Nut Full 3/8" 100Pk	1.00	$6.28	$6.28
Flat Washer 3/8" 100PK	1.00	$5.09	$5.09
Cooling system			$0.00
Peltier Cooler	1.00	$45.00	$45.00
Heat pipe	1.00	$15.00	$15.00
Enclosure			$0.00
Acrylic Cover	1.00	$68.57	$68.57
Aluminum Base plate	1.00	$172.95	$172.95
G. Total Equipment			$493.37
H. Total Project Cost			$843.37

Overall Risk Assessment *(George)*

This is another significant section of the report.

The risk assessment is an important piece of the Conceptual Design Review. This is where you present the information that instills confidence in the upper management, customer and senior engineers that the project is being well managed and is likely to succeed. If there are significant problems with the project, this section identifies the problems and presents the actions that the team will take to mitigate the problem. Leaving risks out or trying to "gloss over" the risks will lead the customer or management to believe that your team does not have a good grasp of the project and does not have a good plan to complete the project.

The parts of risk management that need to be addressed in this section are (1) Technical Risks, (2) Schedule Risks, and (3) Budget Risks. Start with a general paragraph here outlining the status of these risks. Explain the risks in greater detail in the subsections to follow.

Technical Risks (individual)

Technical risks are design, integration and project completion risks that may impact the success of the project. **Technical risk is expected** in any new design. To not have any technical risk is to basically copy what has already been done. Technical risks can include: new or innovative designs that do not have a certainty for success, new technologies being used that are not completely understood, problems with current designs that must be overcome, solutions to design problems that have not been identified, etc.

After a paragraph summarizing the technical risk status of your project, include a subsection for each technical risk you have identified.

Technical Risk 1: <short title of risk>

Description

Describe the risk. Refer to appropriate section of Section 3 as needed for technical details

Probability: < Very Low, Low, Moderate, High, or Very High>

Identify the probability that the risk will impact the project (Very Low, Low, Moderate, High, or Very High). Briefly explain how you determined the probability.

Consequences: <Minor, Moderate, Severe or Catastrophic>

Describe the consequences to your project if this risk were to occur. Identify the impact of this risk occurring to the overall performance of the project.
Briefly explain how you determined the probability.

<u>Strategy</u>

I don't think that we completely answered the question. We are still missing what would we do to handle this risk, our plan? Also we cannot forget to explain how we determine that the probability
- Juan

Technical Risk 2: Datapath Malfunction

○ One technical risk associated with the datapath is a datapath malfunction. The data path may not function or fail to transmit and process data. This malfunction could be **some of the vhdl code being left off** when the current code is copied to add a new data path. The likelihood of this happening is very low because it is very unlikely that code will be copied incorrectly. <Probability: Low>

Maybe we are trying to talk about data errors due to running out of space in the FIFO buffer?
- Juan

Technical Risk 3: Operational Frequency Issues

○ There is a chance that logic locking the frequency at a higher frequency will cause the chip to overheat to fast without a proper cooling system. This would result in a limited amount of testing of the code until the cooling system is implemented. <Probability: High>

○ Another issue during the logic locking process is that the frequency can't actually be raised to the desired 500MHz because the boards capabilities while having such a complex system installed on it might prevent it from reaching this frequency. In this case the project would have to run at the current frequency and have a faster board used for later prototyping of the project in the later phases. <Probability: Moderate>

Technical Risk 4: <short title of risk>

Technical Risk 5: <short title of risk>

Technical Risk 6: <short title of risk>

Schedule Risks(individual)

Schedule risks are those occurrences that directly impact the project being completed on time. These risks can include a number of things including, illnesses, personnel problems, delivery of components, changes to the project requirements, availability of support (mechanical or electrical shops, for example), …

After a paragraph summarizing the schedule risk status of your project, include a subsection for each schedule risk you have identified.

Schedule R isk 1:

<u>Description</u>

Describe the risk.

<u>Probability: < Very Low, Low, Moderate, High, or Very High></u>

Identify the probability that the risk will impact the project (Very Low, Low, Moderate, High, or Very High). Briefly explain how you determined the probability.

<u>Consequences: <Minor, Moderate, Severe or Catastrophic></u>

Describe the consequences to your project if this risk were to occur. Identify the impact of this risk occurring to the overall performance of the project.

<u>Strategy</u>

Describe your strategy to manage this risk. Remember the general categories of strategies that you can use: avoidance, minimization and contingency plans.

Schedule Risk 2: Datapath

One schedule risk associated with the datapath is the likelihood of untimely completion. If another datapath is not added in a timely manner, and new PMT/scintillator arrangement will not be able to be connected to the FEDM. The bit width of the datapaths have [to add room for another datapath] has already been shrunk ahead of schedule. Since this task has been completed early, the likelihood of the task being finished late is very low. <Probability: Very Low>

Schedule Risk 3: <short title of risk>

Budget Risks(individual)

Budget risks are risks that may produce budget overruns. These can include additional support costs, unexpected material or equipment costs, component or system failures, underestimation of costs, …

After a paragraph summarizing the budget risk status of your project, include a subsection for each budget risk you have identified.

Budget Risk 1: <short title of risk>

<u>Description</u>

Describe the risk.

<u>Probability: < Very Low, Low, Moderate, High, or Very High></u>

Identify the probability that the risk will impact the project (Very Low, Low, Moderate, High, or Very High). Briefly explain how you determined the probability.

<u>Consequences: <Minor, Moderate, Severe or Catastrophic></u>

Describe the consequences to your project if this risk were to occur. Identify the impact of this risk occurring to the overall performance of the project.

<u>Strategy</u>

Describe your strategy to manage this risk. Remember the general categories of strategies that you can use: avoidance, minimization and contingency plans.

Budget Risk 2: <short title of risk>

Budget Risk 3: <short title of risk>

Summary of Risk Status (George)

This is a conclusion to your risk assessment. Summarize briefly the status of the risks identified. Leave the audience with the appropriate message: (1) The risks are well understood and managed (ideal), (2) Some risks are a concern, but the team is prepared to manage them (OK), or (3) There are risks that the project team needs help (technical, schedule or budget) to manage (better to ask for help than to have the project fail).

Conclusion (Brian)

Wrap up the message for the report. No new information is included in the conclusion. This is the opportunity to sum up the report and make the case that the project is proceeding well and should be continued.

References

1. J.A. Marin, J.E. Armstrong, and J.L. Kays, "Elements of an Optimal Capstone Design Experience," Journal of Engineering Education, January 1999, pp. 19-22.
2. **...**
3. **...**

Appendices (optional)

You should attach the supporting documents and material that are relevant to your project.

Calculating the Internal Run time counter of the FEDM:

$$2^{56} \cdot T \cdot \frac{1\,minute}{60\,seconds} \cdot \frac{1\,hour}{60\,minutes} \cdot \frac{1\,day}{24\,hours} = \text{Number of Days of Operation before overflow}$$

T = period of the FEDM code