COSMICi: High Energy Particle Detector

Group 6:
Aarmondas Walker - Team Leader
George Chakhtoura - Co- Team Leader
Samad Nurideen - Secretary
Brian Kirkland - Treasurer
Juan Calderin
Michael Dean

Problem Statement

- Phase I
  - The detectors will send voltage pulses through coaxial cables to an FPGA for digitization.
  - This data will be wirelessly transmitted to the kiosk.
  - Bit width reduction to make room for new inputs
  - Desired frequency of final design will be 500MHz
  - The system components will have a mounted enclosure
  - Detectors will be installed at the Challenger Learning Center

Intended Users

- **Intended Users**
  - Will be implemented in learning centers
    - Challenger Learning Center
    - High Schools
    - Libraries
    - Astrophysicists
- **Intended Use**
  - Capture Cosmic Ray Shower events
  - Triangulate location
  - Contribute Data to MARIACHI (Mixed Apparatus for Radar Investigation of Atmospheric Cosmic-rays of High Ionization) data sets

Logic Locking of High-Speed Components and Bit-Width Reduction

- Michael Dean
- Computer & Electrical Engineering

Performance Assessment: After Bit-Width Reduction

- The internal timing counter was 64-bits wide, giving over 10 years data values
- This value was reduced to 56-bits and still give 4.5 years
- The system memory improvements after reduction:

Before:

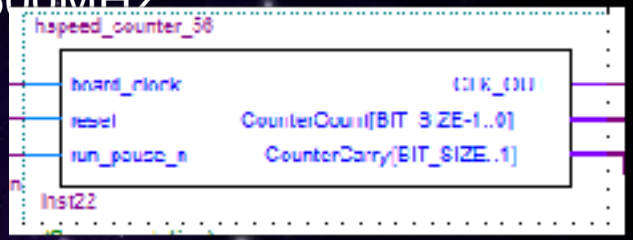
- Slow Corner Fmax for high-speed counter: 211.28MHz
- Logic Utilization: 24,314 / 27,104 (90%) = 2,790 remaining
- Dedicated logic registers used: 21,878 / 27,104 (81%) = 5,226 remaining
- M512 blocks: 193/202 (96%) = 9 remaining
- M4K blocks: 144/144 (100%) = 0 remaining
- M-RAM blocks: 1/1 (100%) = 0 remaining

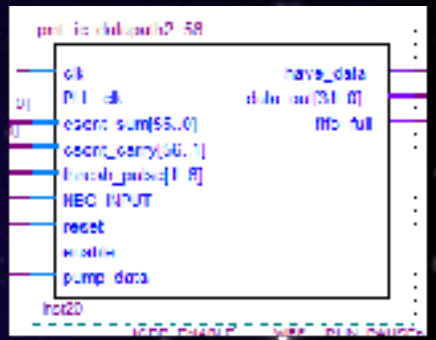
After:

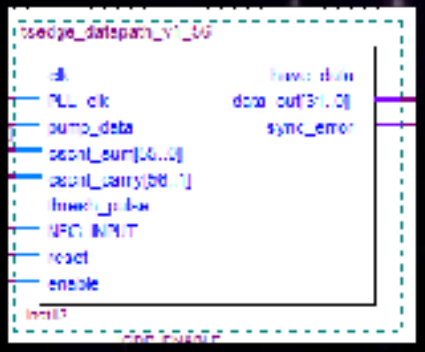
- Slow Corner Fmax for high-speed counter: 213.13 MHz (slightly better)
- Logic Utilization: 22,007 / 27,104 (81%) = 5,097 remaining (almost 2x better)
- Dedicated logic registers used: 19,463 / 27,104 (67%) = 7,641 remaining
- M512 blocks: 188/202 (93%) = 24 remaining (more tha n 2x better)
- M4K blocks: 144/144 (100%) = 0 remaining (same)
- M-RAM blocks: 1/1 (100%) = 0 remaining (same)

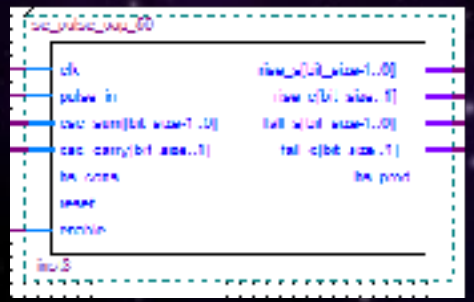
Logic Lock:
Components of the System

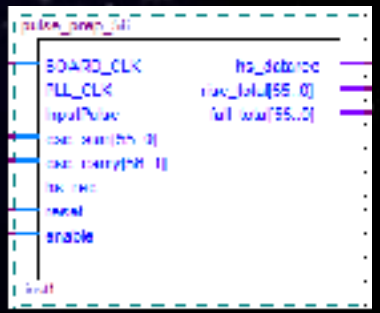
- The high-speed components in this system, those using the Phase-Locked Loop (PLL) line, will be sped up from their current 211 MHz to 500MHz
- High-speed time-counter
- Input Capture Datapaths
- Photo-multiplier Tube Pulse Digitizer
- Pulseform Capture Datapath
- Pulse Prep
- SE Pulse Cap





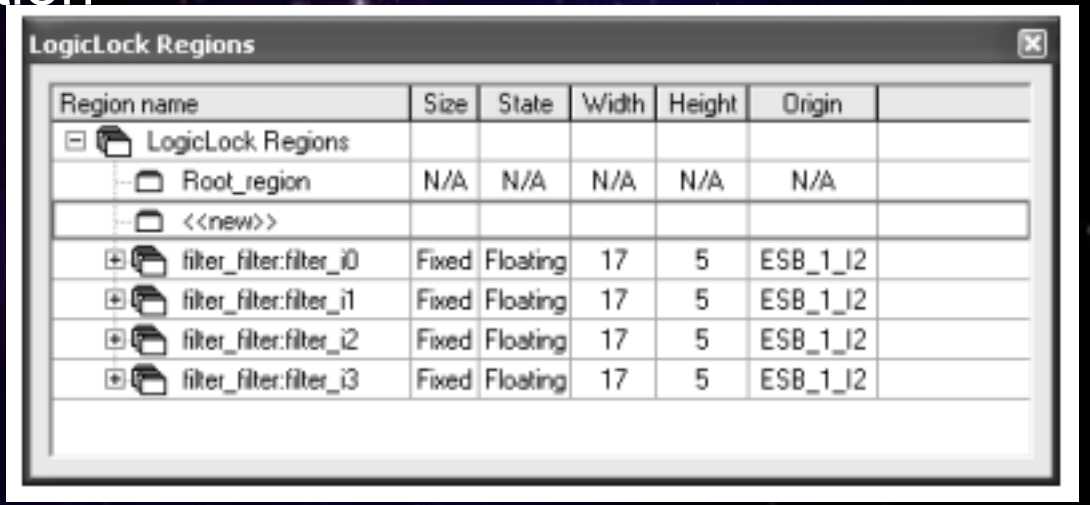






Logic Lock
Logic Locking Methodology

- In order to increase the Front-End Digitizer Module (FEDM) to an operational frequency of 500MHz Quartus' Logic Locking feature will be utilized
- This will be applied to the high-speed components to allow us to specify multiple properties about the logic locked region
- Logic Locking has several settings:
  - State - Floating or Locked
  - Size - Auto or Fixed
  - Reserved - On/Off -
  - Enforcement - Hard or Soft
  - Origin - Floorplan Location

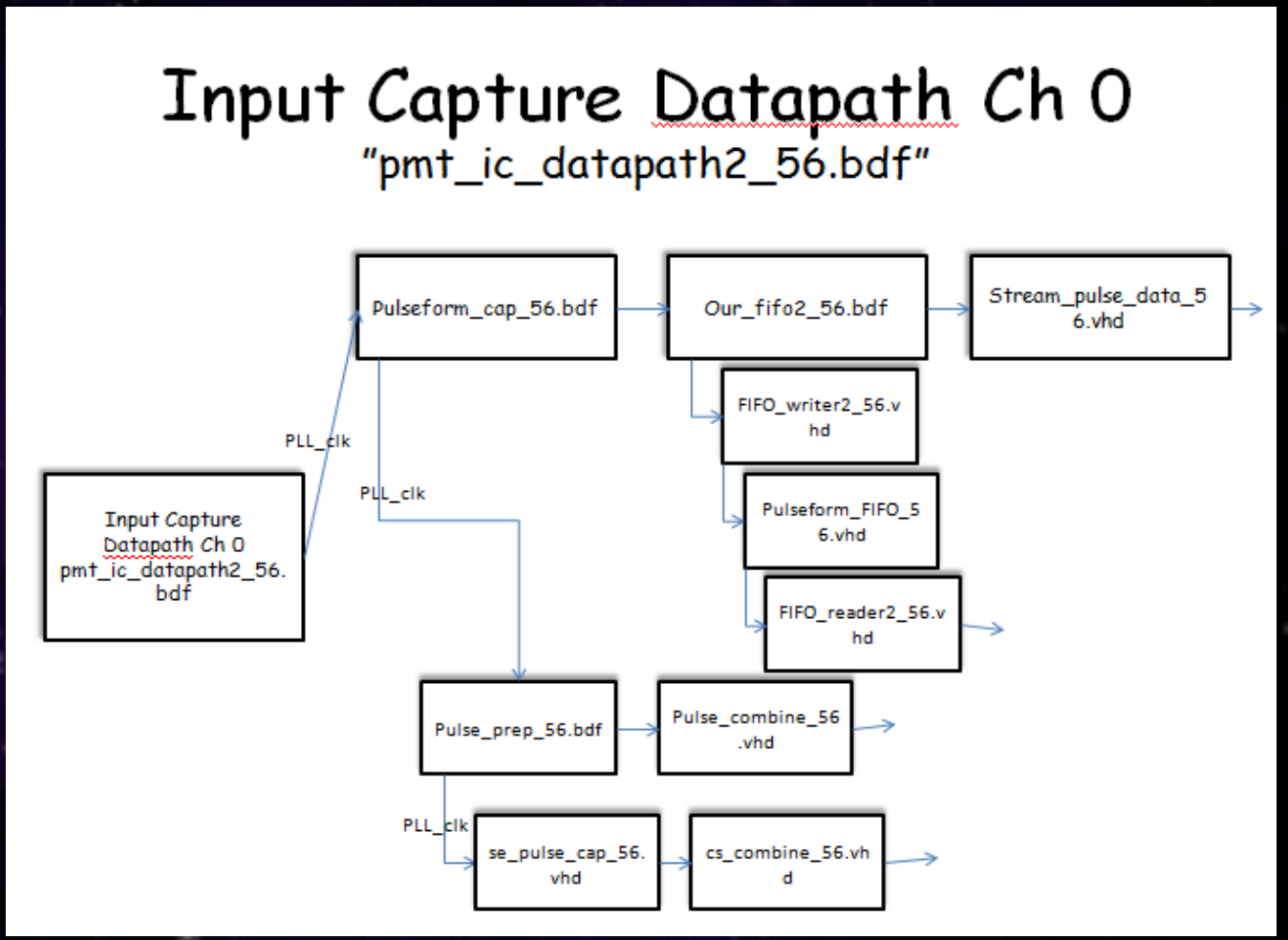


Logic Lock Application

- All components utilizing the Pll_clock line will be locked
- How to apply it:
  - State - Floating or Locked
    - Floating regions allow Quartus to determine the appropriate location of the block, while Locked uses a user defined location
  - Size - Auto or Fixed
    - Auto lets Quartus handle sizing while Fixed uses user defined sizing and shaping
  - Reserved - On/Off -
    - Enabling allows Quartus to utilize resources from this region for entities not assigned to this region
  - Enforcement - Hard or Soft -
    - Soft enforcement allows deference of the region to timing constraints, allowing entities to leave region if performance is improved. Hard enforcement does not abide by the relocation of entities
  - Origin - Location on Floorplan -
    - Defines where the logic lock region is at

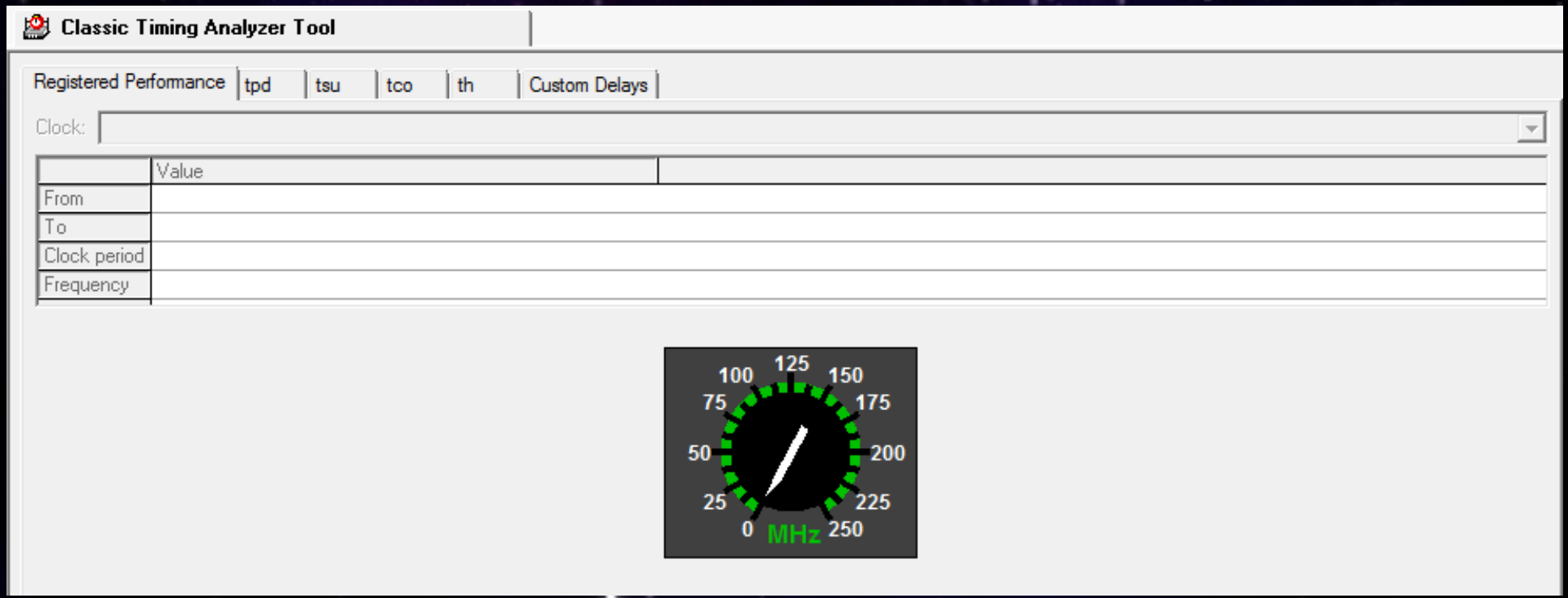
Logic Lock:
Components Utilizing PLL_Clock

Below is a graphical image of how the ICDP utilizes the PLL_clk line



Circuit Speed: Testing Methodolgy

- To test the circuit speed the Classic Timing Analyzer Tool will be used
- After compiling the project this feature can be used to get an estimate on where the cirouit board is currently operating with the FEDM design



Timing-Sync Datapaths: VHDL

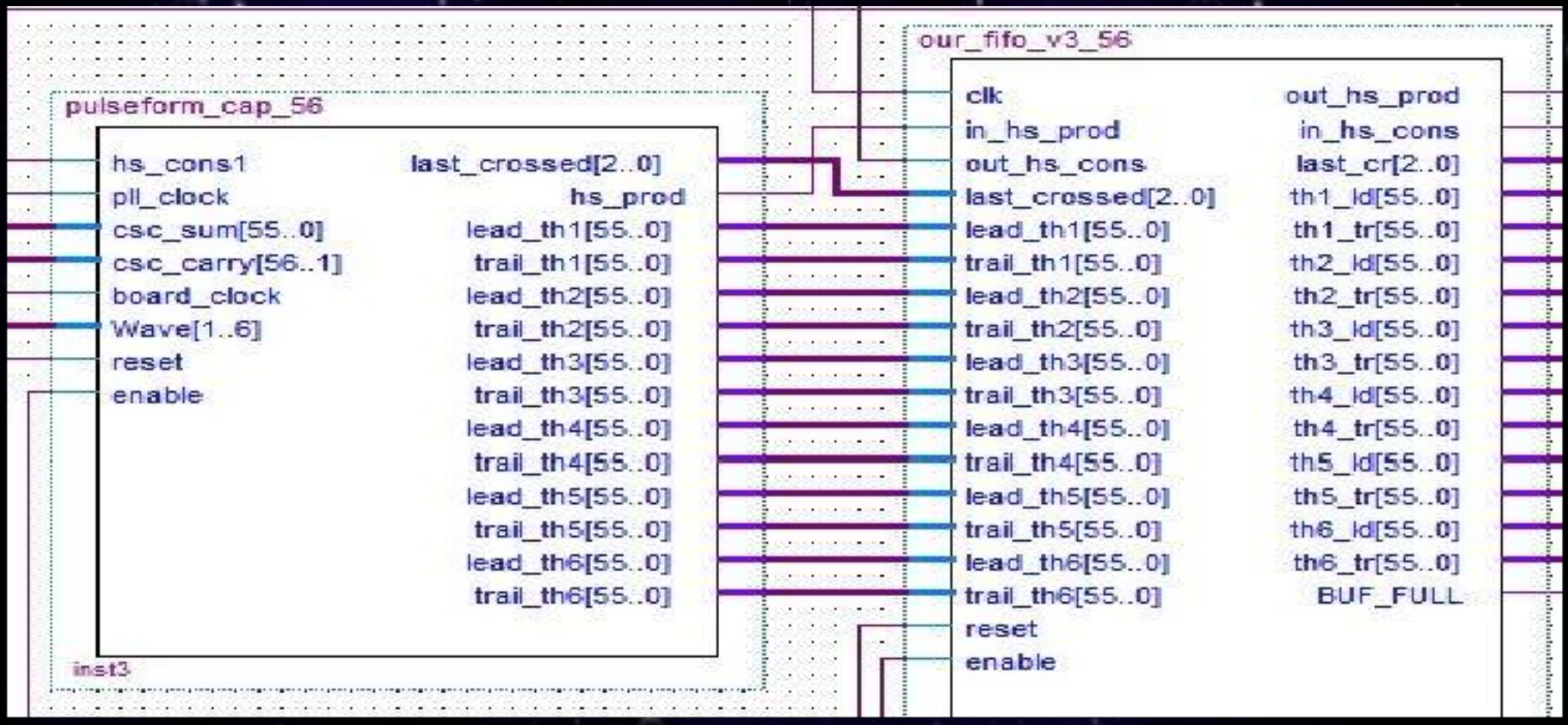
- Aarmondas Walker
- Computer Engineering

Timing-Sync Datapaths: VHDL

- The TSDP is being modified to disregard the voltage thresholds 2-6. It is now only concerned with the first voltage threshold. This module will only be triggered by the rising edge of the threshold.

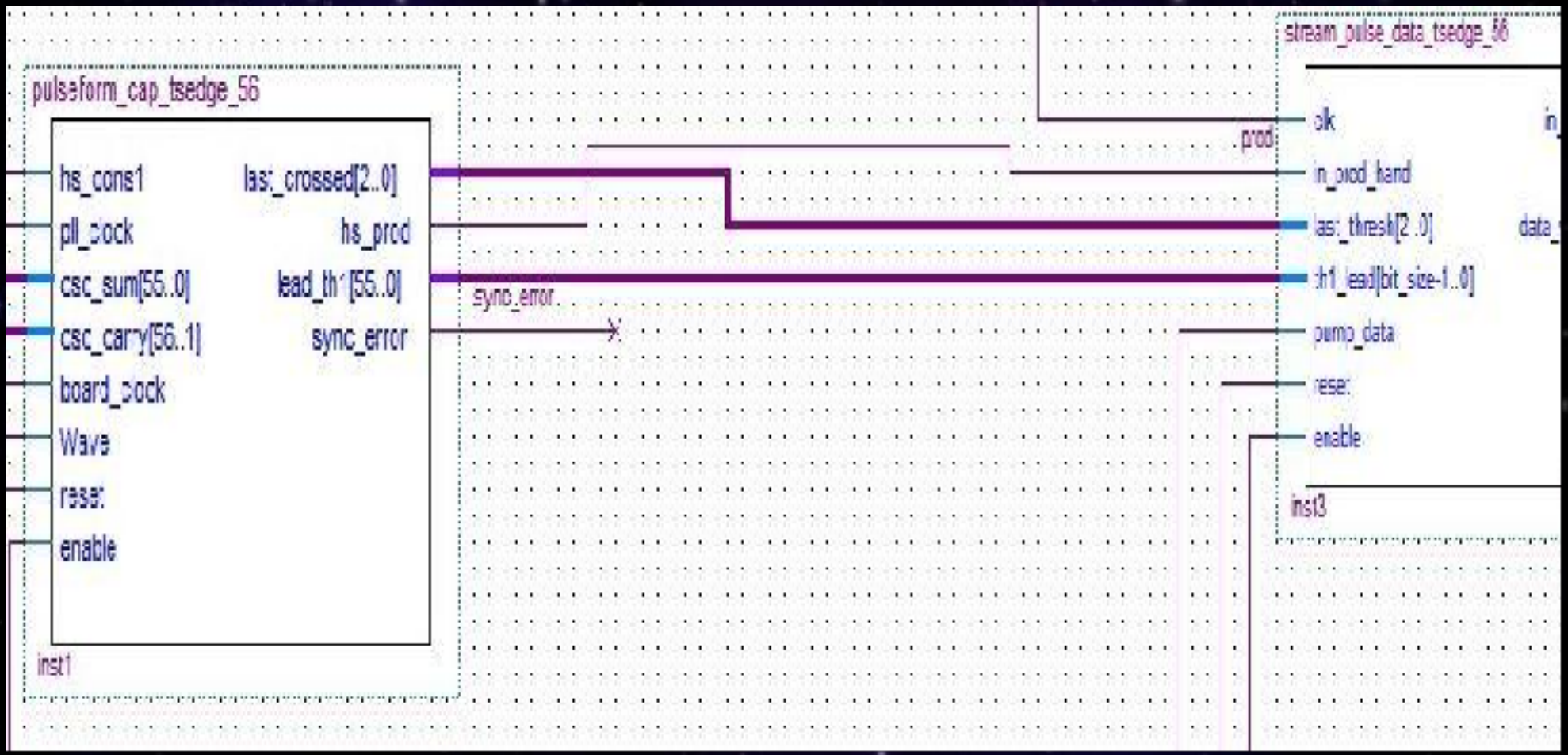
Timing-Sync Datapaths: VHDL

Before Modifying



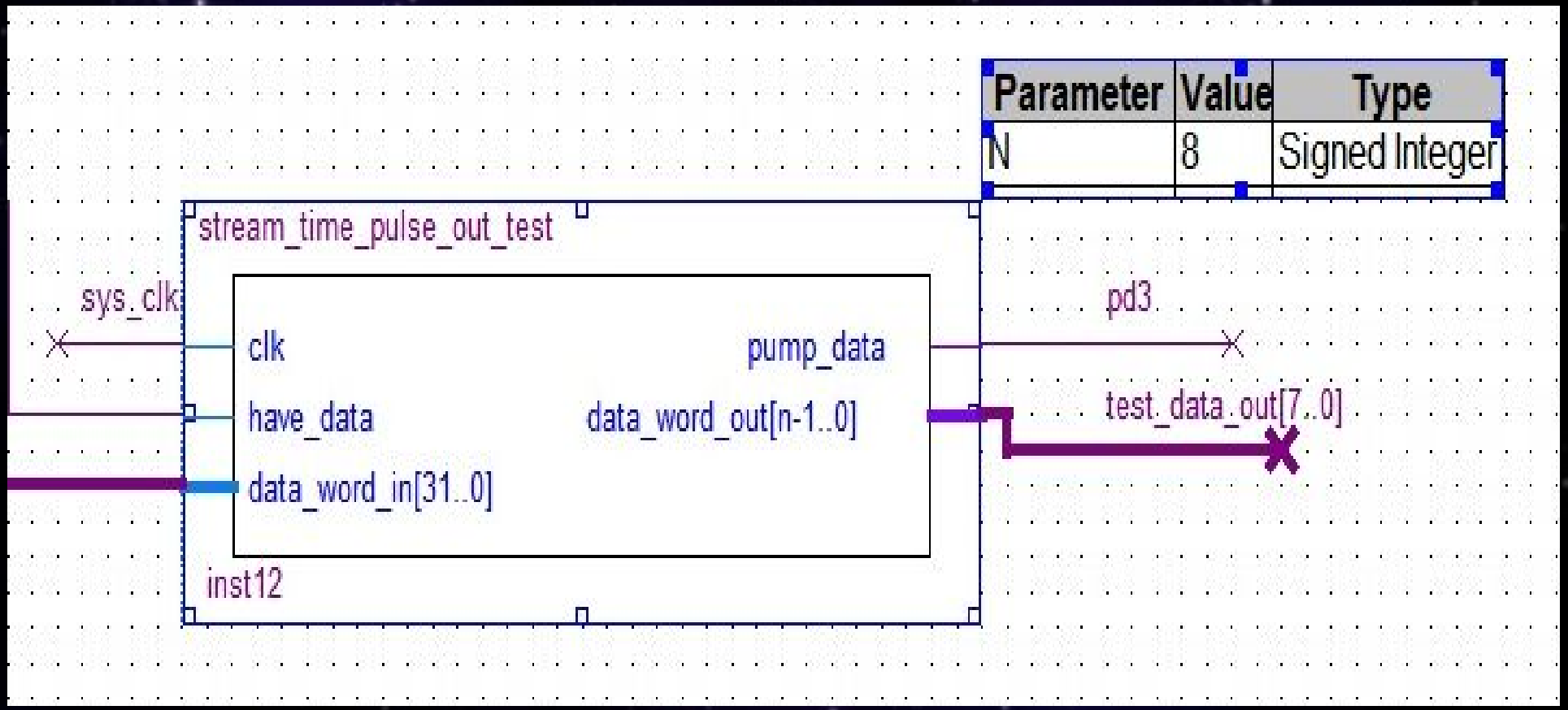
Timing-Sync Datapaths: VHDL

After Modifying



Timing-Sync Datapaths: Testing

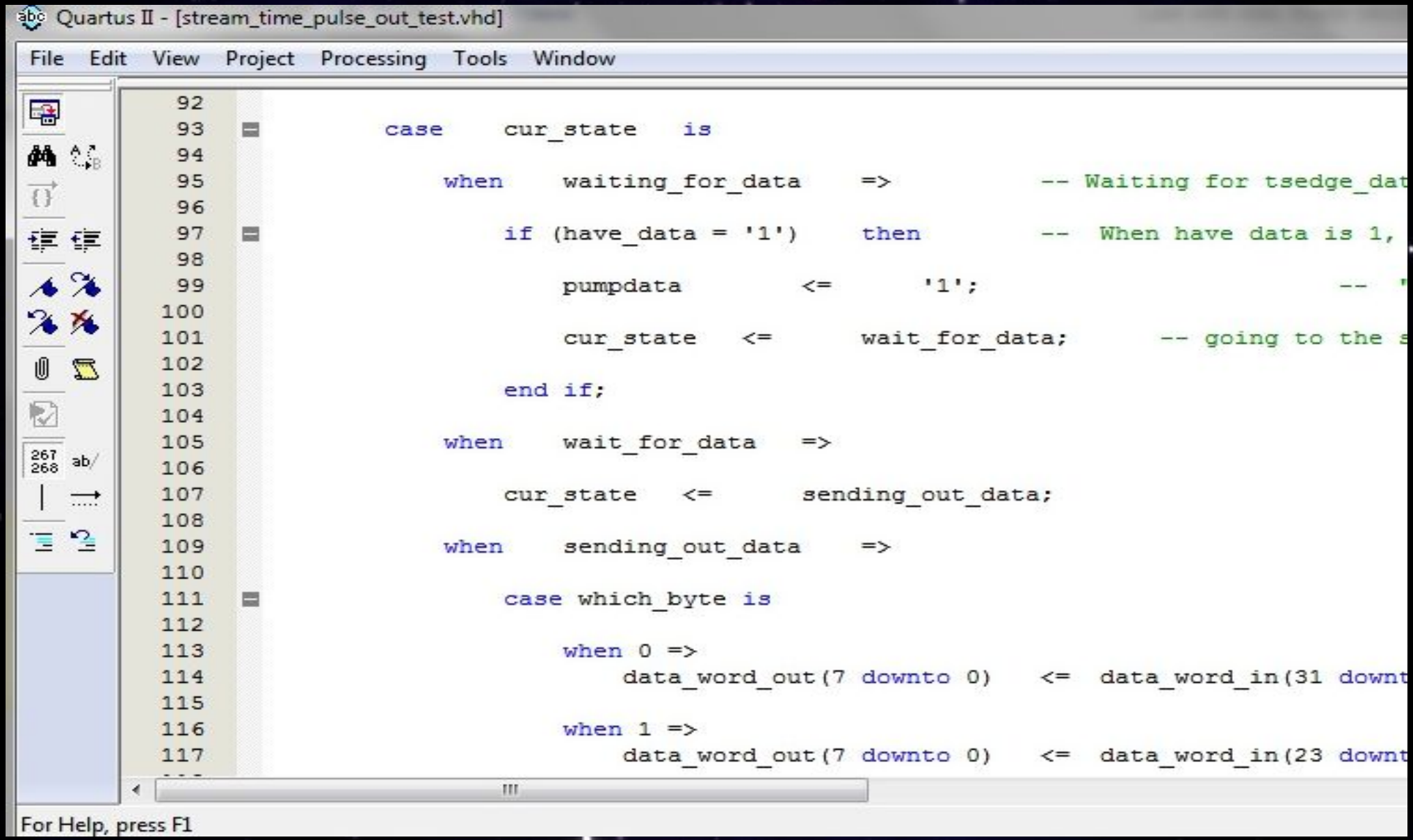
Module used for testing



Timing-Sync Datapaths: Testing (cont.)

- Has an input of one word
  - Acquires two words from input
  - data is output sequentially

Timing-Sync Datapaths: Testing (cont.)

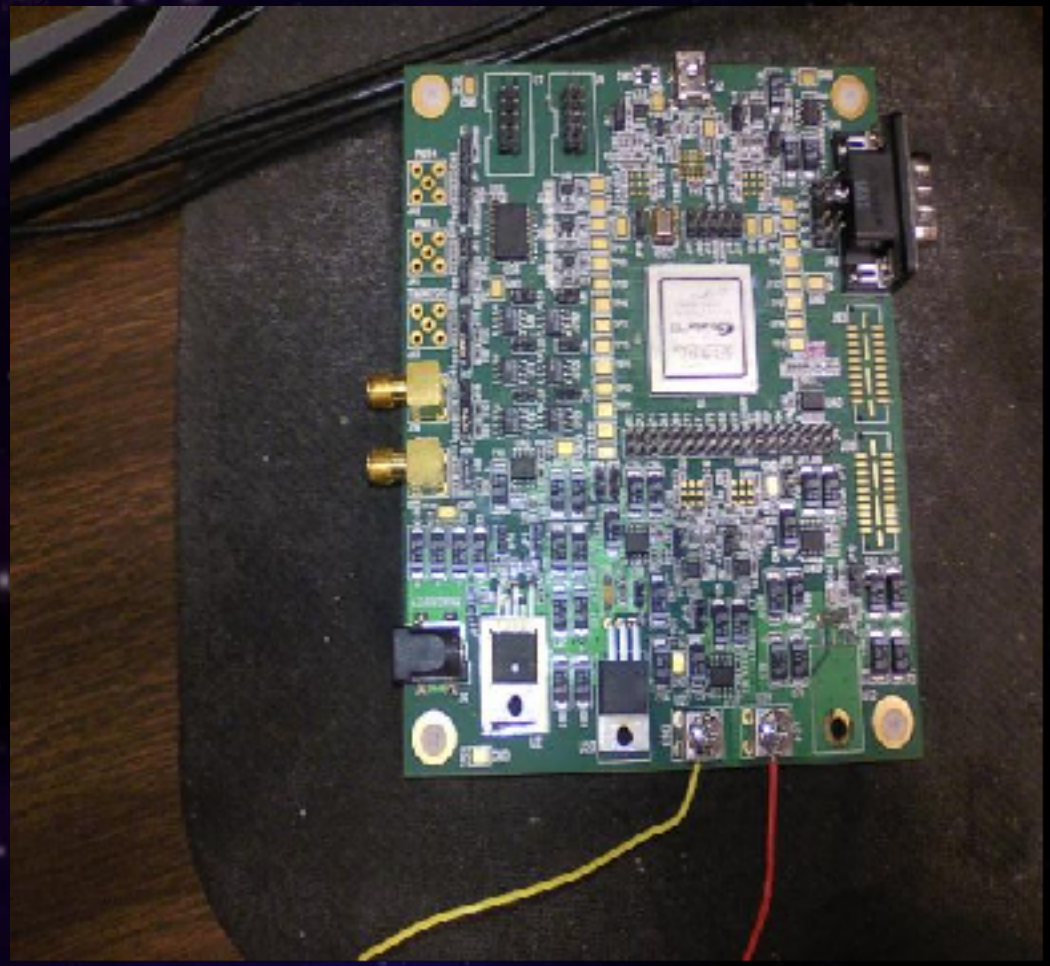


Front end digitizer module(FEDM)

- Juan Calderin
- Computer Engineering

Front End Digitizer Module

- **Purpose:**
- To digitalize the analog signals from the cosmic ray detectors and have them ready for the server to process them.
- Mainly written in C and VHDL



Front End Digitizer Module (updates)

A new "driver" has been added to the firmware to handle the new timing sync data path.

Front End Digitizer Module
Function Declarations

```
extern  void    tsdp_init(void);    // To be called by main().

extern  void    tsdp_reset(void);   // Resets the state of the timing input capture data path
                                    // ensuring stored data is cleared.

extern  void    tsdp_run(void);     // Enable the timing-input-capture datapath to start or continue running.
extern  void    tsdp_pause(void);   // Pause the operation of the input-capture datapath. (Lower TSDP enable.)

    // Event handlers for the input-capture interrupts.  Called from interrupt.c.

extern  void    tsdp_handle_have_data   (void); // Call TSDP_have_data isr. No paramaters necessary.
                                                // (as opposed to icdp; have_data could go low for
                                                //  three different channels)

extern  void    tsdp_handle_sync_error  (void); // Call timing sync_error
```

Test Plan

Using debug statements (diagnostics function) to check that correct timing data is being sent and processed.

```
/*
    //|------------------------------------------------------------------------
    //|
    //|     tcdp_diagnostics()                  |          [private procedure]
    //|
    //|         Verbosely display a bunch of descriptive information
    //|         about a pulse on the JTAG debug port (stdout).
    //|
    //|vvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvv
```

Central Server

- **Purpose**: to process and graphically display the data coming wirelessly from the FPGA.
  - Written in Python
  - The server will be running in the kiosk computer located in the Challenger Learning Center.

Central Server (updates)
Behind schedule

- **Task(s):**
  - Analysis & visualization of incoming pulses
  - Database storage of pulse data for offline analysis
- **Information Display**: We can use the VPython libraries for 3D display.Integrate it with Google Sky using the Google Earth API.

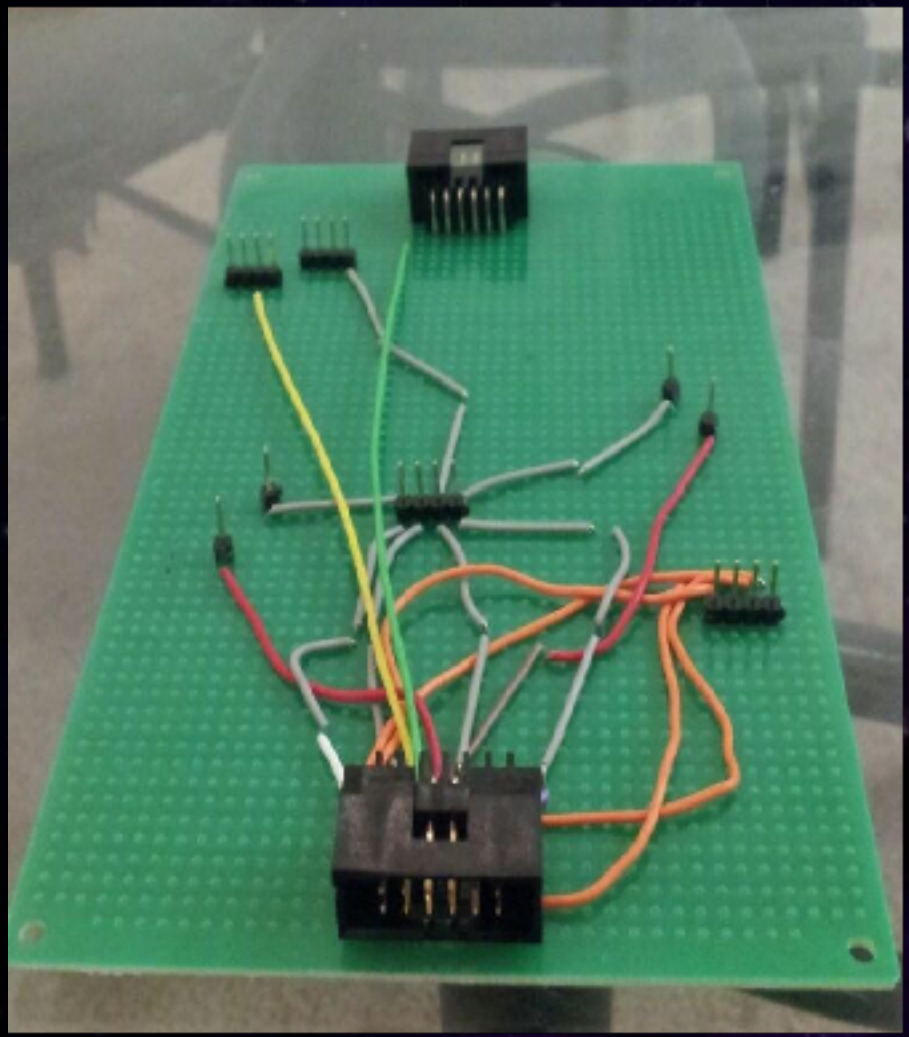
Test Plan

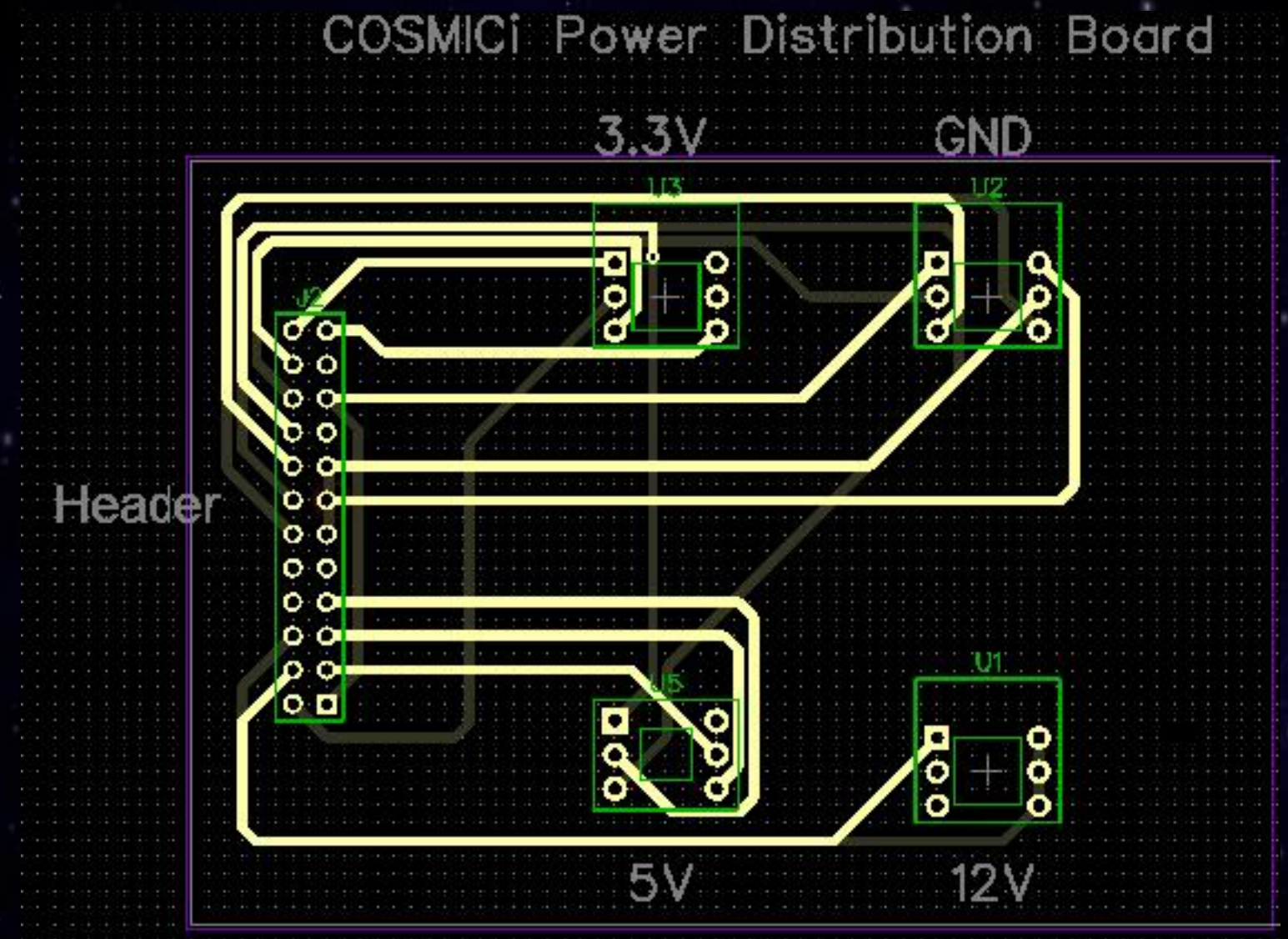
- **Long term testing to check that data has been received.**

Power Supply

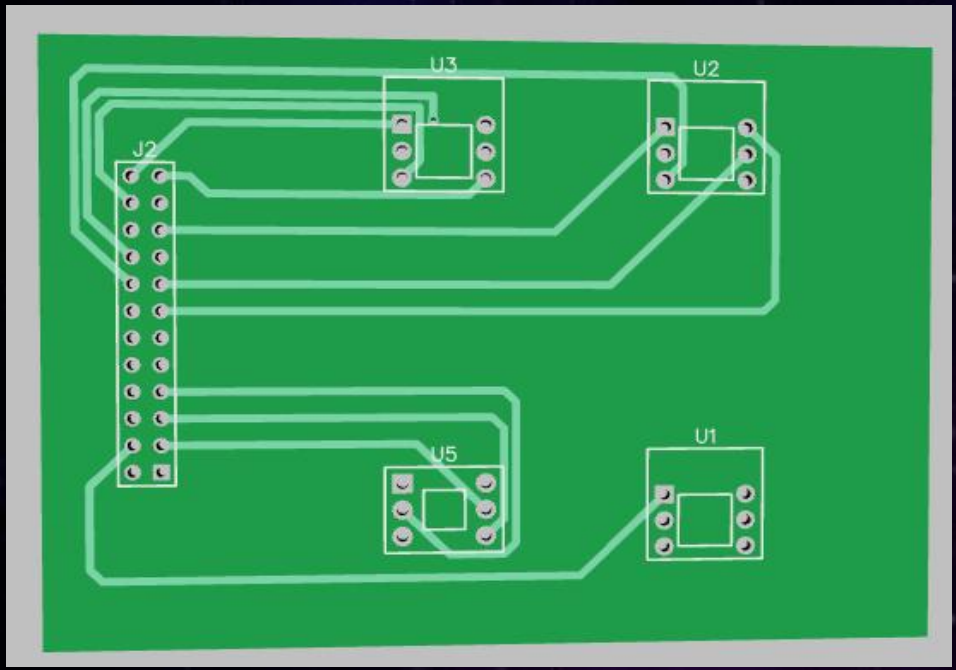
- Samad Nurideen
- Electrical Engineering

Powering Components

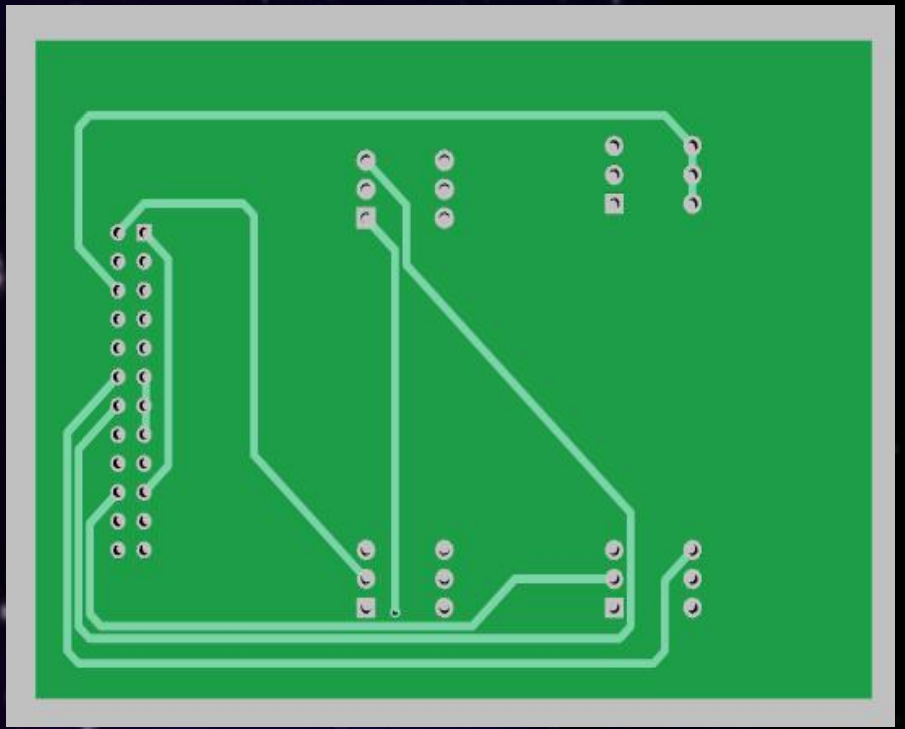



COSMICi Power Distribution Board
3.3V
GND
U3
U2
J2
Header
J5
U1
5V
12V

TOP



BOTTOM



Power Supply % Completion

Power Supply – 80% of Overall Task Goal

Subtasks:

Power FEDM – 10% Complete 10/5/11
Power CTU – 10% Complete 10/19/11
Power both CTU and FEDM – 70% 0%
Provide Power for detectors – 10% 0%
POWER SUPPLY GOAL IS 20% COMPLETE

Battery – 20% of Overall Task Goal

Subtasks:

Research – 30 % Complete 10/20/11
Order Parts – 10% 5%
Implement – 40% 10%
Test – 40% 10%

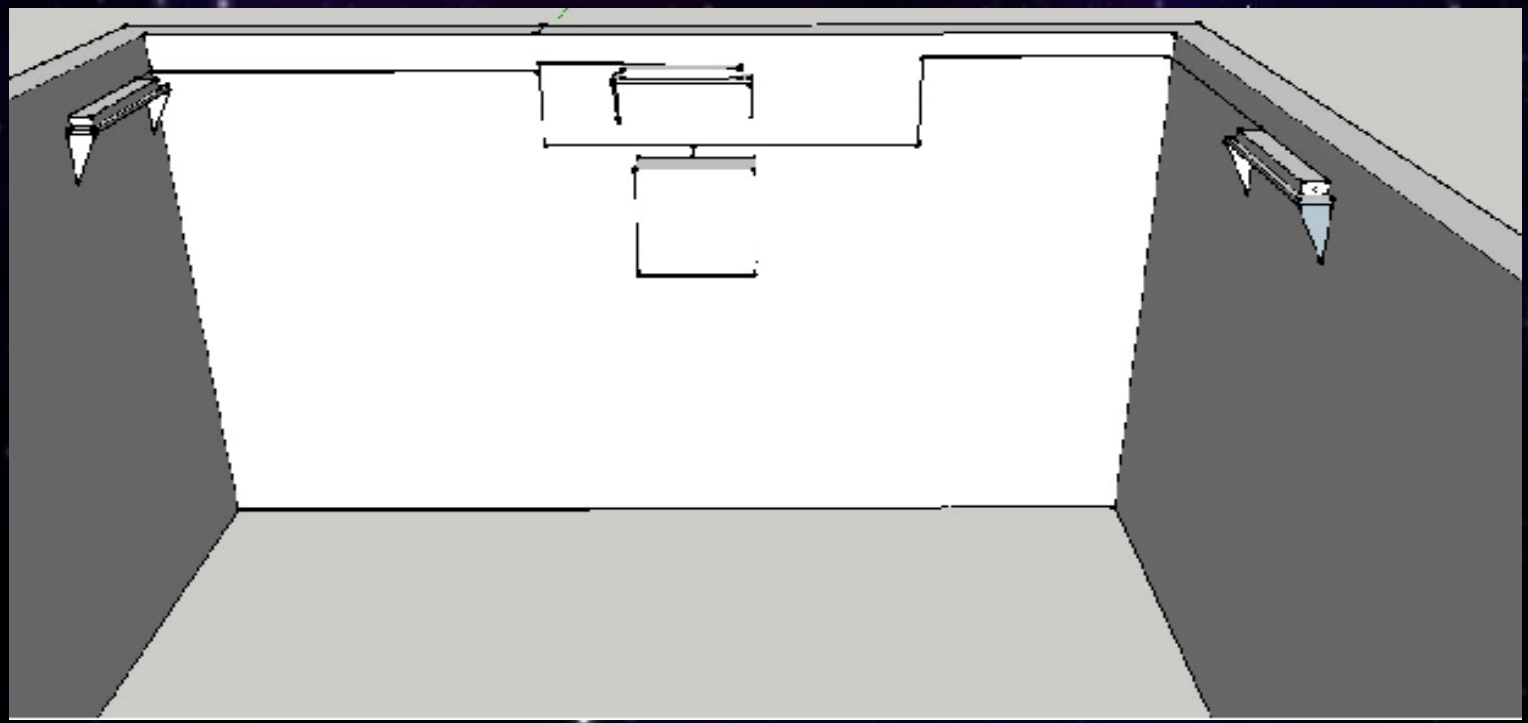
55 % OF BATTERY GOAL IS COMPLETE

Structural Support
&
Enclosure Design

- Brian Kirkland
- Mechanical Engineering

New Structural Design

- 2 I Beam connected support structures.
  - For single detector and component enclosure.
- Two Shelving unit support structures.
  - For remaining two detectors.



Structural % Completion

Scintillator Support – 75% of Overall Task Goal

Subtasks:

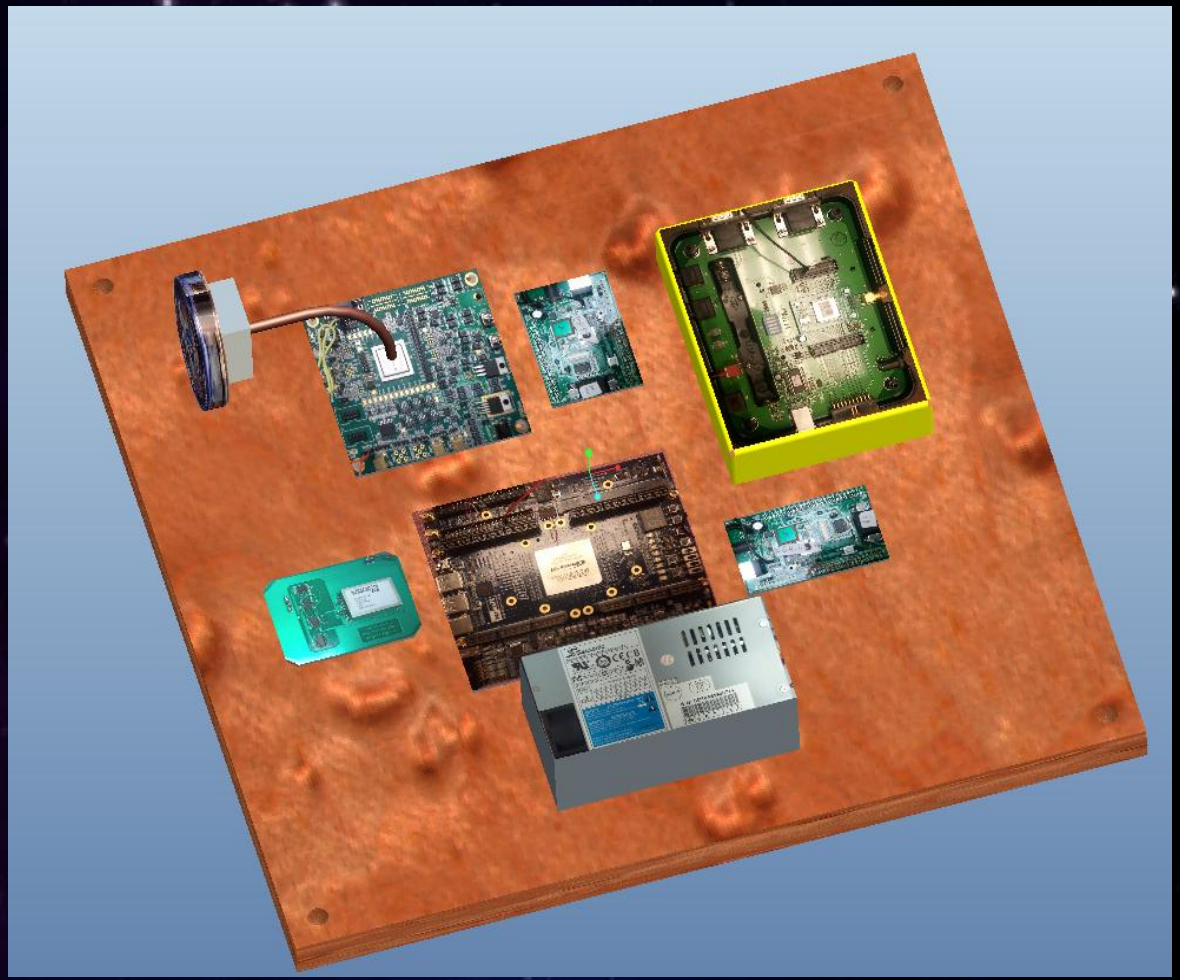
- Scintillator Measurement – 10% Complete 10/07/11
- Room Measurement– 10% Complete 10/14/11
- Fastening Method Analysis – 50% Complete 11/05/11
- Part Ordering-20% TBD
- Design Implementation – 10% TBD

70% OF OVERALL STRUCTURAL SUPPORT GOAL COMPLETE

Enclosure: Summary

- Enclosure built to house system hardware components.
- Singular location for all needed accessible components.
- Protection from physical shock, dust,and debris.

- Comprised of two pieces.
  - Base plate
  - Plastic cover



Enclosure System Test Fit

- Wired circuit boards to be fitted to base-plate.
  - White chalk outline on base plate
    - Relative position
      - Boards
      - Cooling system
      - Power supply
      - Fasteners
  - Use relative positions to finalize board design
- Attach to I beam support structure

Enclosure testing

- Failure test
  - Determine if base plate can hold prescribed weight without failing(cracking or deflecting > 5mm)
    - Using 80 lbs of weight centrally loaded board was tested and did not fail Feb 6th
    - Board was supported on four corners as would be with structural supports

Enclosure % Completion

Subtasks:

- **Base plate:** 45% Complete
  - Designing : 31.5%
  - Machining: 13.5%
- **Clear Cover:** 45% 20%
  - Designing: 27%
  - Machining: 9%
  - Fabrication: 9%
- **Assembly**: 10 % 0%
  - Fabrication: 10%

- **45% OF OVERALL ENCLOSURE GOAL COMPLETE**

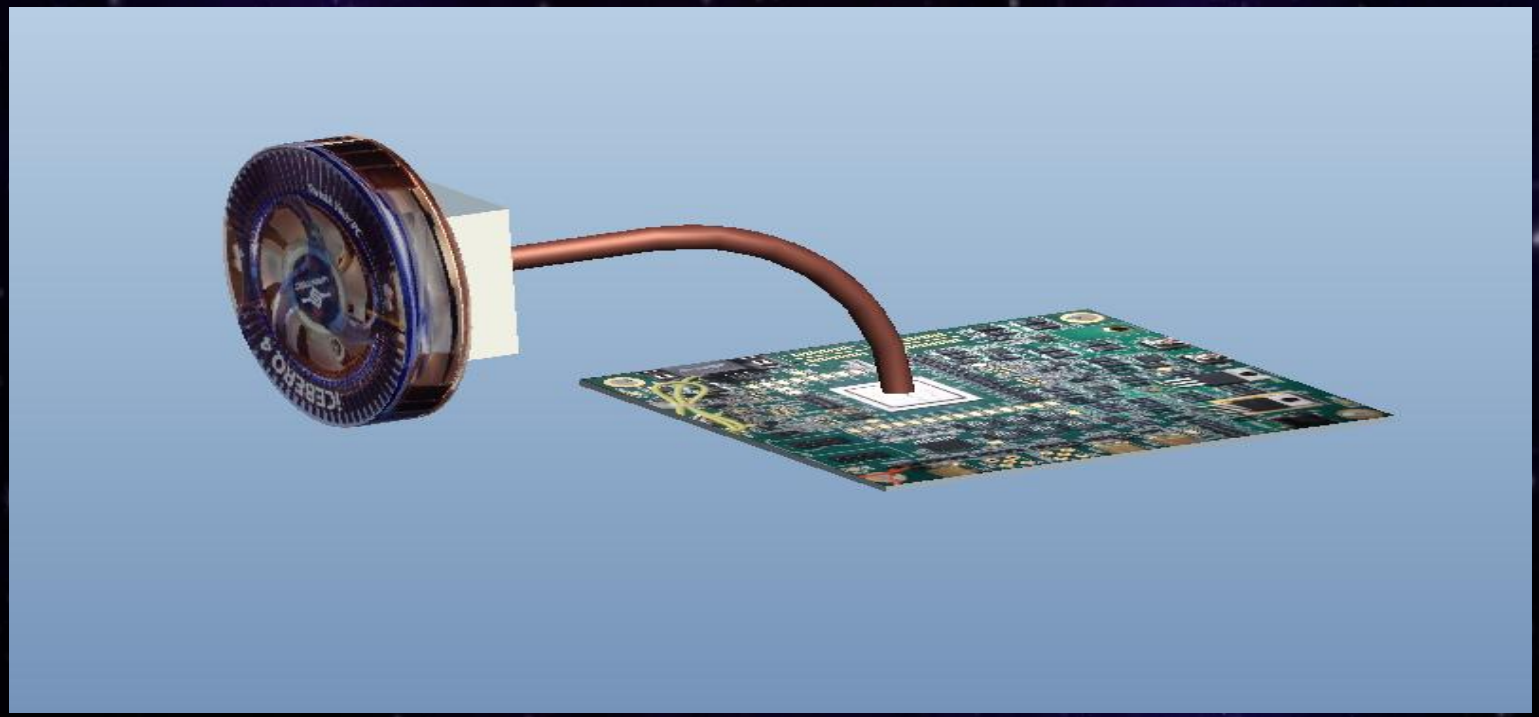
Cooling System

- George Chakhtoura
- Mechanical Engineering

Cooling System

Components include:

- Polyurathane Coated Copper Heat Transfer Rod
- Thermoelctirc Cooler Plate
- Copper Fin Heat SInk Fan Assembly



Cooling System Cont...

- Copper has 2X the thermal conductivity of Aluminum and 3X that of Stainless Steel, thus the material change for the heat pipe and fins.
- The new heat sink fan assembly will provide suffcient air flow as well as serve for aesthetic pleasing.

$Q=k*a*(Thot-Tcold)/d$
Established Heat Rate (from current system) Q= 126.563 W
Cross Sectional Area a= $5cm^2$
Desired Rod Length d= 8.4cm
Thermal Conductivity of Copper k= 401 W/m*K
Running Temperature (Thot) Thot= 53°C (326K)
Desired Running Temp(Tcold) Tcold= 0°C (273K)

Updated Specs With New Thermoelectric Cooler
Q=70W
=>Desired Rod Length d=3.3cm

Cooling System Components And Testing

- The figure below illustrates a mock representation of the Copper heat transfer rod and Infarred Thermometer that will be used during testing.
  - Rubberized coating test failed.
    - Condensation build up
  - System Test 1
    - Feb. 13
    - Using current thermoelectric cooler.
  - System Test 2
    - Feb 29 - Mar 2
    - Using new thermoelectric cooler

Testing Risk Assessment: Cooling System

- Possible dislodgment of heat transfer rod: Low
  - Countermeasures: The cooling system will be mounted and supported inside the enclosure to provide additional stability.
- Possible occurrence of condensation: Extremely Low
  - Countermeasures: Thicken 2mm polyurathane insulation wall.
- Possibility of not reaching optimal temp: Extremely Low
  - Countermeasures: Use current thermoelectric cooler.

Cooling % Completion

Subtasks:

Temperature Measurements of Chip and Board –5%	Complete 11/07/11
Physical Measurements of all Boards – 5%	Complete 10/20/11
Peltier cooler, fins, and fan cad design – 15%	Complete 11/08/11
Solve Condensation Issue –10%	Complete 11/08/11
Provide heat equations showing chip temp – 30%	Complete 11/28/11
Order correct size peltier cooler, fins and fan –5%	Complete 02/01/12
Connect cooling system to structure–5%	0%
Test for Issues–25%	0%

70 % COOLING SYSTEM GOAL IS COMPLETE

General Information

Aarmondas Walker
Computer Engineering
Brian Kirkland
Mechanical Engineer

Expected Deliverables

- Phase I:
  - COSMICi System will detect UHECR from at least 3 scintillator devices
  - The system will operate at a frequency of 500mhz
  - The direction and source of the cosmic ray shower will be displayed to the user in the kiosk computer in the form of a sky map (possibly physics dept. task).
  - A power source will be configured to supply all the components
  - An enclosure will protect the circuit boards
  - A Cooling System will maintain the FPGA chip at 0 C and the circuit boards at room temperature
  - A structural design will support the scintillator-detectors and the enclosure

Budget

D. Expense	Quantity	Unit Price $	Total $
Equipment			
Structural Support			
Beam Clamp 3/8"	4	2.39	9.56
Threaded Rod 3/8"	4	8.89	35.56
Hex Nut Full 3/8" 100PK	1	6.28	6.28
Flat Washer 3/8" 100 PK	1	5.09	5.09
Cooling System			
Peltier Cooler	2	7.50	13.00
Heat Pipe	1	41.00	41.00
Enclosure			
Acrylic Cover	1	68.57	68.57
Birch Plywood Baseplate	1	9.99	9.99
Total Equipment Cost			210.32
Total Project Cost			**210.32**

Overall Risk Assessment

- Technical Risks
  - Structural System Malfunction
  - Datapath Malfunction
  - Operational Frequency Issues
- Schedule Risks
  - Datapath
  - Enclosure Completion
- Budget Risks
  - Underestimation of Costs/Parts
  - Not Enough Funding
- Other Risks
  - Engineers Getting Sick
    - Hindering Completion of Portion
  - Engineers Dropping Out of Project

Gantt Chart - Update

	Task Name	Duratio	Start	Finish	Predecessors	R
7	Visit Challenger Learning Center	1 day	Tue 10/25/11	Tue 10/25/11		
8	MECHANICAL ENGINEERING SIDE	87 days?	Mon 10/3/11	Fri 1/27/12		
9	STRUCTURAL SUPPORT	87 days?	Mon 10/3/11	Fri 1/27/12		J
18	ENCLOSURE DESIGN	31 days?	Fri 11/4/11	Wed 12/14/11		E
26	Cooling Ststem Design	61 days?	Mon 11/7/11	Fri 1/27/12		C
35	ECE SIDE	83 days?	Mon 10/3/11	Mon 1/23/12		
36	Increase Input Datapaths	77 days?	Tue 10/11/11	Mon 1/23/12		A
43	Circuit Speed Optimization	19 days?	Mon 11/21/11	Thu 12/15/11	39	J
48	Power Supply	82 days?	Mon 10/3/11	Fri 1/20/12		S
56	Detailed Design Report	11 days?	Sat 11/5/11	Thu 11/17/11		
62	Python Server	53 days?	Wed 1/4/12	Fri 3/16/12		
63	Server Coding Workshop	3 days?	Wed 1/4/12	Fri 1/6/12		
64	Determine Tasks/Split Task	1 day?	Fri 1/13/12	Fri 1/13/12	63	
65	Research/Determine Solution	1 day?	Fri 1/27/12	Fri 1/27/12	64	
66	Coding	35 days?	Mon 1/30/12	Fri 3/16/12	65	

Gantt Chart

Completed Tasks - ECE

35		**ECE SIDE**	**83 days?**	**Mon 10/3/11**	**Mon 1/23/12**
36		**Increase Input Datapaths**	**77 days?**	**Tue 10/11/11**	**Mon 1/23/12**
37	✓	Review current code	9 days	Tue 10/11/11	Fri 10/21/11
38	✓	Creat plan to decrease width	3 days	Fri 10/21/11	Tue 10/25/11
39	✓	Decrease Width	4 days	Wed 10/26/11	Mon 10/31/11
40	✓	Add Input	32 days?	Thu 12/1/11	Fri 1/13/12
41	✓	Check for errors	4 days?	Mon 1/16/12	Thu 1/19/12
48		**Power Supply**	**82 days?**	**Mon 10/3/11**	**Fri 1/20/12**
49	✓	Provide Power for FEDM	3 days	Mon 10/3/11	Wed 10/5/11
50	✓	Alternative Power Solutions	13 days	Tue 11/15/11	Thu 12/1/11
51	✓	Research Solution	3 days	Tue 12/6/11	Thu 12/8/11
52	✓	Feasibility Study	3 days	Tue 12/6/11	Thu 12/8/11

Completed Tasks -ME

8		**MECHANICAL ENGINEERING SIDE**	**87 days?**	**Mon 10/3/11**	**Fri 1/27/12**
9		**STRUCTURAL SUPPORT**	**87 days?**	**Mon 10/3/11**	**Fri 1/27/12**
10	✓	Idea Generation Phase	8 days	Mon 10/3/11	Wed 10/12/11
11	✓	Idea Evaluation	1 day	Tue 10/18/11	Tue 10/18/11
12	✓	Feasible Approaches	1 day	Wed 11/9/11	Wed 11/9/11
18		**ENCLOSURE DESIGN**	**31 days?**	**Fri 11/4/11**	**Wed 12/14/11**
19	✓	Get PCB sizes	1 day	Fri 11/4/11	Fri 11/4/11
20	✓	Get approx cooling system size	1 day	Fri 11/11/11	Fri 11/11/11
21	✓	Design system	9 days	Sat 11/12/11	Wed 11/23/11
22	✓	Material Selection	7 days?	Sat 11/12/11	Mon 11/21/11
26		**Cooling Ststem Design**	**61 days?**	**Mon 11/7/11**	**Fri 1/27/12**
27	✓	Get board Measurments	1 day?	Mon 11/7/11	Mon 11/7/11
28	✓	Get FPGA chip max running temp	1 day?	Mon 11/7/11	Mon 11/7/11
29	✓	Design Sstem	2 days?	Mon 11/14/11	Tue 11/15/11
30	✓	Find best metal for conduction/ material selection	1 day?	Mon 11/14/11	Mon 11/14/11
31	✓	Design Calculations	5 days?	Mon 11/14/11	Fri 11/18/11
32	✓	Order Materials	1 day?	Mon 12/5/11	Mon 12/5/11

Presentaion Dedicated to J. Pascal Desmangles

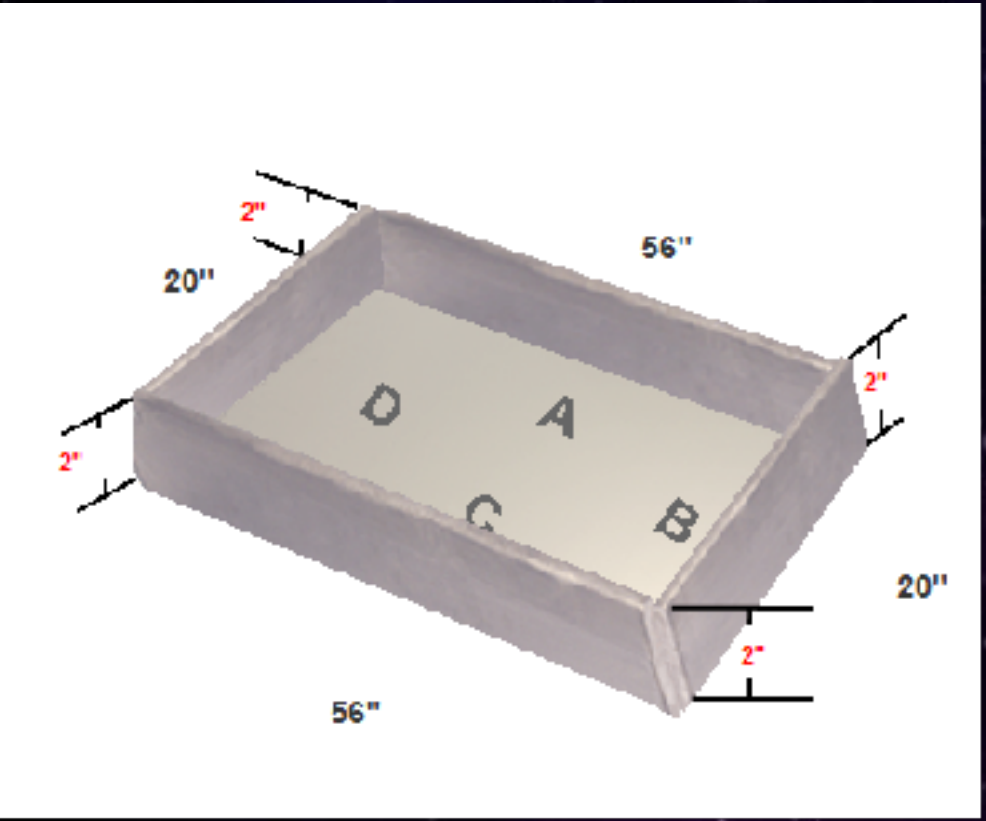
Bright Spirit, Brilliant Mind, Devoted Teammate

Questions?

Works Cited

- Ashby, Michael F. *Strengh vs Density*. Digital image. *Grantadesign.com*. Web. 3 Nov. 2011. <http://www.grantadesign.com/download/charts/new_strength_density.pdf>
- *Cosmicrays2*. Digital image. *Http://www.aspera-eu.org*. Web. 3 Nov. 2011. <http://www.aspera-eu.org/images/stories/Media/MEDIAPICTURES/HR/cosmicrays2.jpg>.
- Cosmic Inquirer blog by Miichael P. Frank.
- .

Appendix



Detector Support Design

Material Selection

- **Need To use plots from Ashby's textbook to find the best material**
  - **Material Index**
    - **Shows which guide lines to use**
    - **Gives an idea of which plots to use**
- **Must use Modulus vs. Relative cost plot**
  - **Relative cost**
    - **Necessary to correct values and remove influence of inflation and units of currency**

$$C_{v,r} = \frac{\frac{Cost_{material\ selection}}{kg} * Density\ of\ material\ selection}{\frac{Cost_{steel}}{kg} * Density\ of\ mild\ steel\ rod}$$

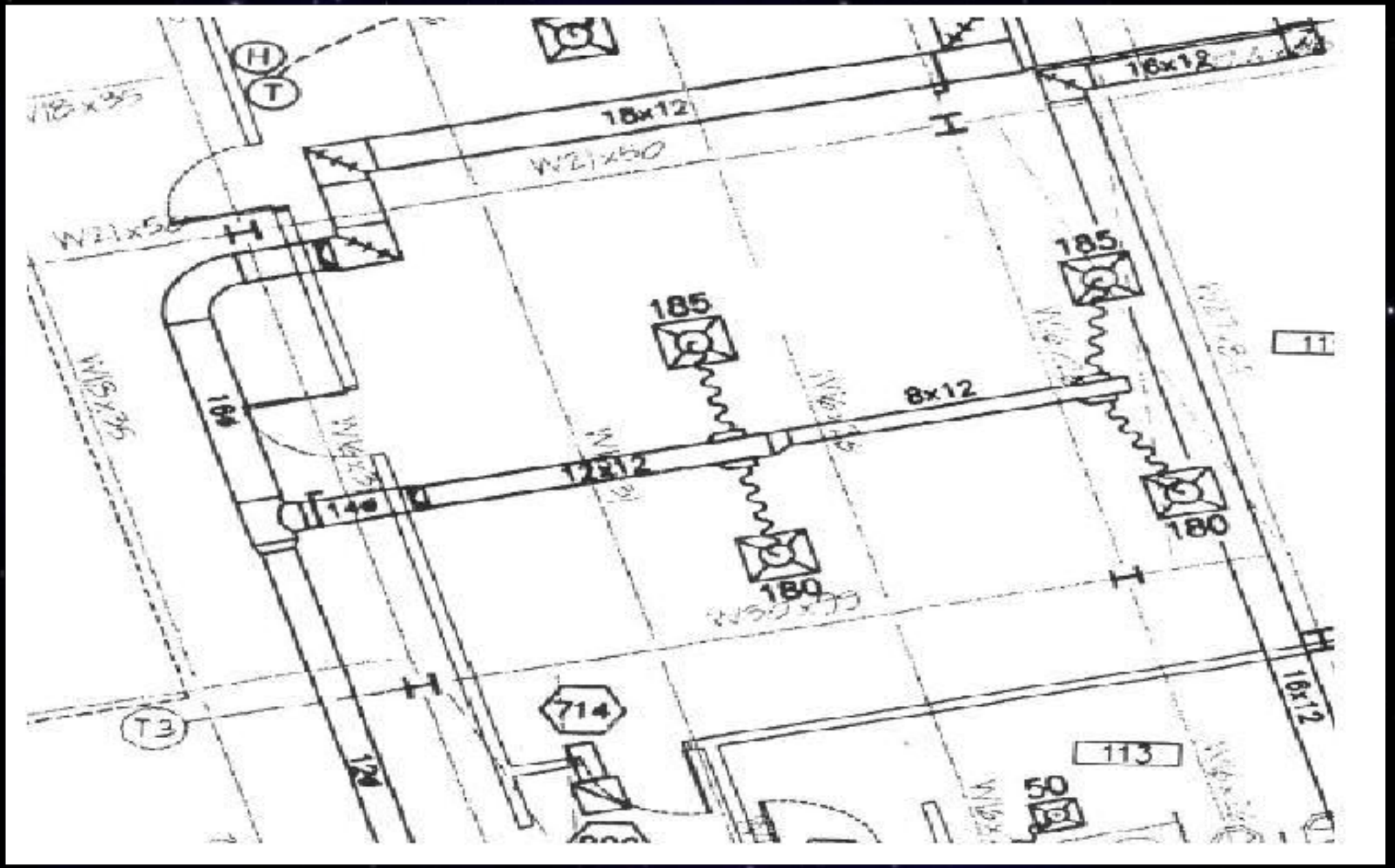
Process selection

- Wood is a natural material
- Birch plywood is prefabricated in sheets with specific thickness and sizes
- The only Real feasible option for processing wood is conventional machining
- The finishing process will involve sanding and coating with varnish to bring out the natural aesthetics of the wood grain

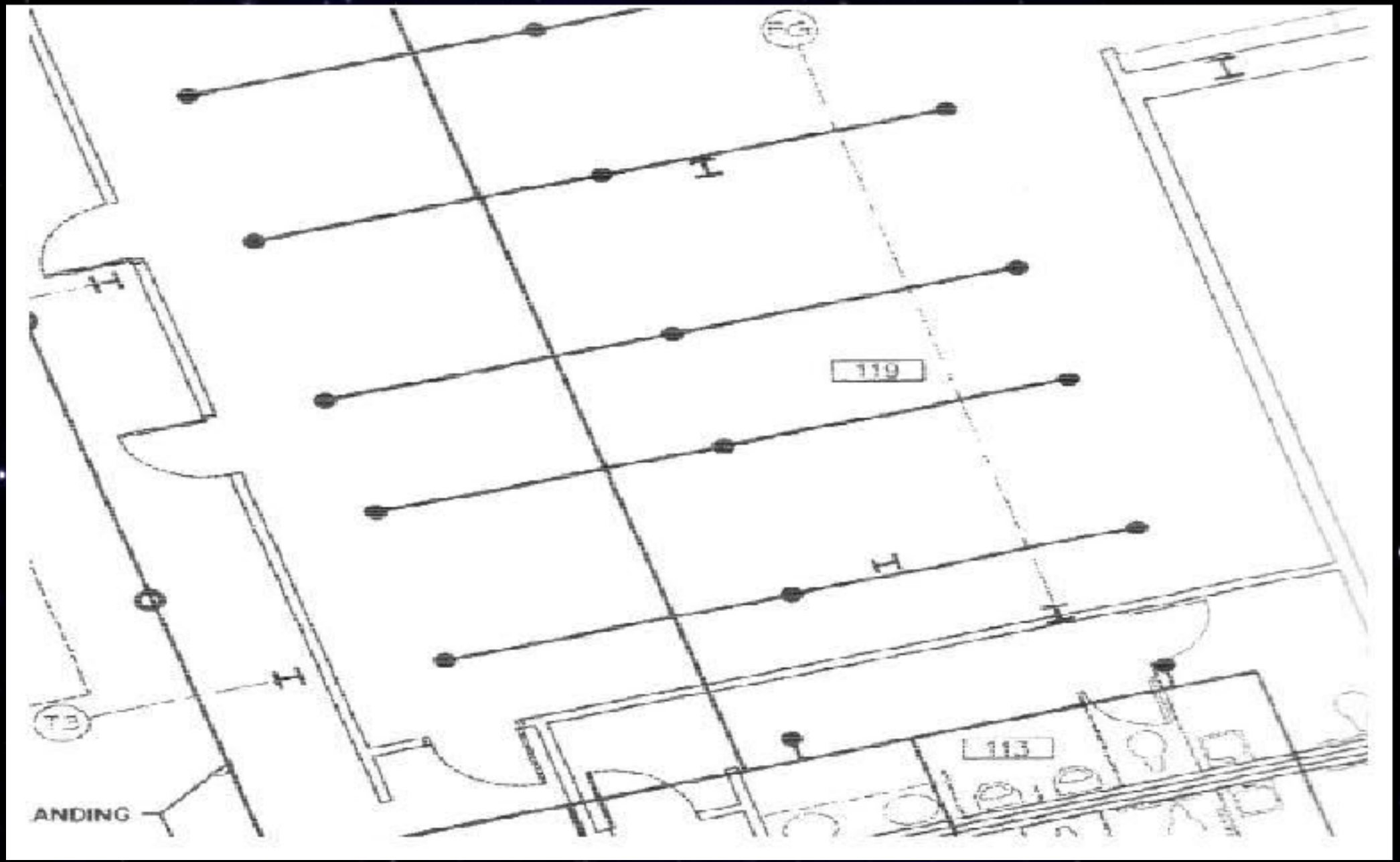
Material Choice: References

- *Aluminum Plate*. Digital image. *Made-in-china.com*. Web. 29 Nov. 2011. <http: //image.made-in- china.com/2f0j00bBpEIOzJZvuV/Fireproof-Aluminum- Plate. jpg>.
- Ashby, M. F. *Materials Selection in Mechanical Design*. Burlington, MA: Butterworth- Heinemann, 2011. Print.
- *Baltic Birch Plywood*. Digital image. Web. 29 Nov. 2011. <http://images.rockler. com/rockler/images/63388-01- 200.jpg>.
- "MDF Board FAQ - Tutorial." *DIY Audio & Video - FAQs, Tutorials, and Calculators for Speaker Boxes, Crossovers, Filters, Wiring and More*. Web. 29 Nov. 2011. <http://www.diyaudioandvideo.com/FAQ/MDF/>.

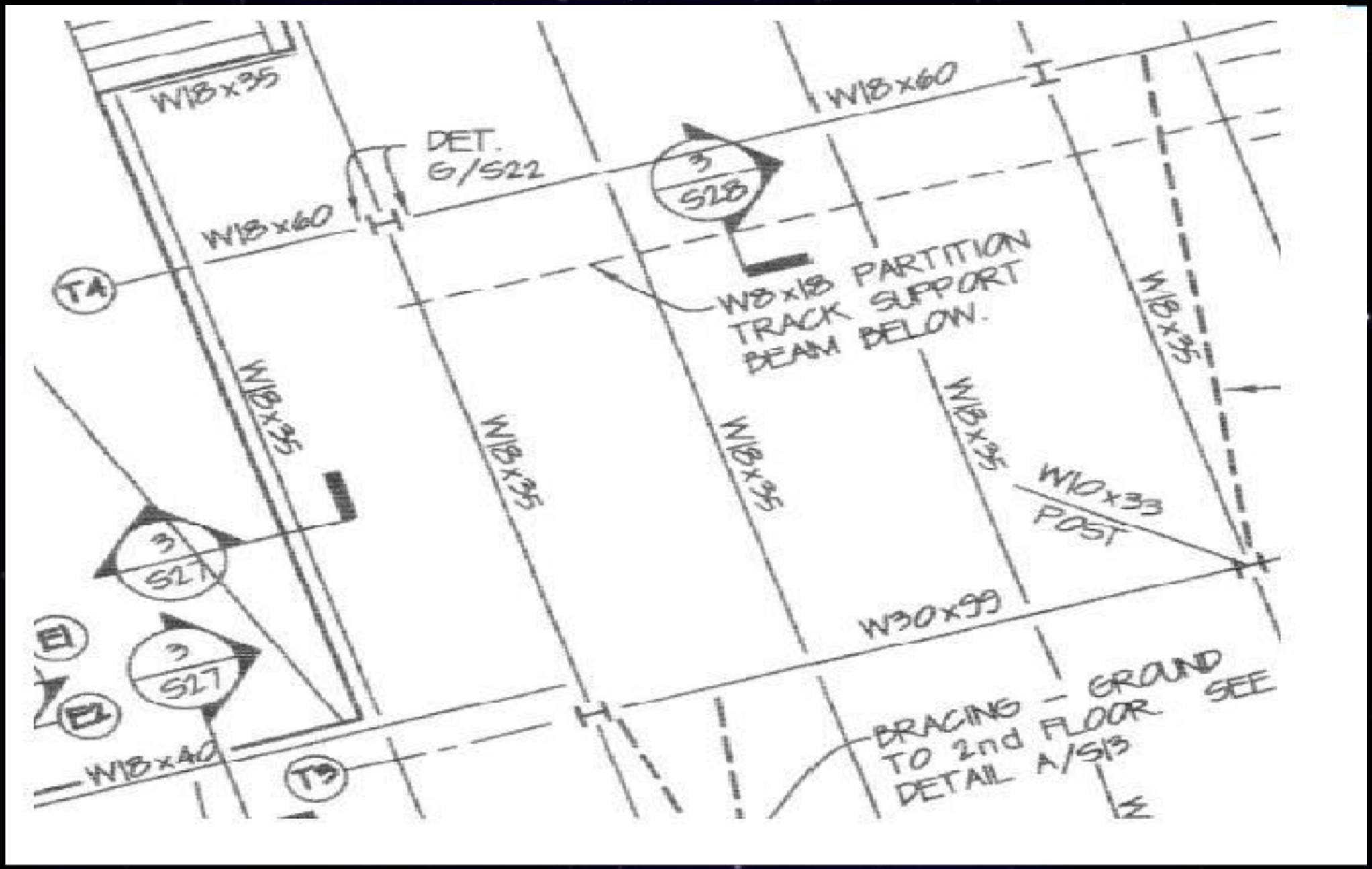
Drawings (vent)



Drawings (sprinkler)



Drawings (iBeam)



Drawings (electrical)