FAMU-FSU College of Engineering
Department of Electrical and Computer Engineering

EEL4911C – ECE Senior Design Project I

CONCEPTUAL DESIGN REVIEW

Project title: **COSMICi**

Team #: 06

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February 02, 2012

Executive Summary

The COSMICi Project aims to create a large distributed network of localized, wireless cosmic-ray sensor sub-networks. Many of the sensor networks will be stationed in learning centers such as: the Challenger Learning Center (CLC) in Tallahassee, Florida, high schools, and science museums. The detector arrangement will ultimately be available to the public - hobbyists and cosmic questers (individuals that interested in the fields of astronomy, astrophysics, cosmology and particle physics) in particular.

These scintillator sensors will detect showers of particles in the air that are generated by ultra-high energy cosmic ray particles. The light emitted from the high-energy shower when they pass through the scintillator will then be amplified using a Photo Multiplier Tube (PMT) and then transmitted to an FPGA board.

The FPGA board will then digitize the voltage pulses from the scintillator detectors and wirelessly transmit this data to a central server (a kiosk). During the initial design phase, the information will be transmitted to a computer, when the product is ready for installation at the CLC, the data will be transmitted computer that is setup at a public kiosk. The central server will then log and triangulate the source of the cosmic ray shower events. The information will then be displayed to an end-user.

Eventually the data collected by the scintillator sensors will be contributed to MARIACHI (Mixed Apparatus for Radar Investigation of Cosmic-rays of High Ionization) data sets which will help astrophysicists have more information about the occurrence of cosmic ray showers events and be able to tell where high-energy primary cosmic-ray particles come from.

The project is divided between the Mechanical Engineering (ME) discipline and the Electrical and Computer Engineering (ECE) discipline. On the ECE side - Michael Dean has shrunk the bit width of the input capture datapaths to make room for another datapath. He will also work towards getting the FPGA to operate at 500 MHz. Aarmondas Walker is helping to creat a new, simpler input capture datapath for registering timing sync pulse arrivals. Juan Calderin is also working on the timing sync datapath and a visualization feature on the central server.

On the ME side – Brian Kirkland and George Chakhtoura will come up with a structural support solution to mount the scintillators and the enclosure. Brian Kirkland will fabricate an enclosure for all the circuit boards and cooling system. George Chakhtoura will create a new cooling system solution that will cool the FPGA more effectively.

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1. Introduction

The COSMICi Project's design phase is approaching conceptual completion. Changes are being made in the software so that the hardware can perform at a higher operational circuit speed. The software team is working on reducing component blocks and firmware code while the cooling system team is tailoring a Peltier cooler to the needs of the system based on measured data. A power source has been devised and is currently being set up to power all the boards and three scintillator detectors. The central server configuration is nearly 35% complete – the visualization feature will be added. An enclosure to house all circuit boards is being designed protect the electronics from outside disturbances while still allowing them to be viewed by the public eye. In order to install the system in the CLC a structural support design is being finalized and parts will be ordered soon.

1.1 Acknowledgements

The design team would like to thank Dr. Frank and Dr. O'Neal for the help that they have given to the project and all of the advising. Also, the team would like to ackowledge David Grosby and Darryl McGowan for their initial codeing of the Front-End Digitizer Module Gelware.

1.2 Problem Statement

The objective of this project is to install a fully functional cosmic ray detection network at the Challenger Learning Center in downtown Tallahassee, Florida. The system will be installed according to a configuration that allows it to triangulate the origin of a cosmic ray shower and display the results on a computer screen.

General Solution Approach

Fully Functional

The engineering team will have to address a few system issues before the final installation. The team will have to solve the following: slow processing speed, number of data inputs, data display, FPGA cooling system, protective enclosure for circuit boards, and structural supports for all detectors.

Configuration

The detectors will ideally be placed 30 ft apart in a roughly triangular configuration and communicate via coaxial cables to a main processing unit (FEDM), which will use a wireless module to wirelessly send the data to the kiosk(central server) for processing and visualization.

In a later stage (Phase II) each detector will have its own processing unit (FPGA board) and wirelessly send the data to the kiosk. This configuration will require the design and

implementation of an optical synchronizer that will ensure that the detectors have the same time reference point (master clock).

1.3 Operating Environment

These devices will be installed in learning zones (such as the Challenger Learning Center – Tallahassee, Florida), schools and other academic learning facilities. As such, they will need to have durable cases that can prevent any damage to the components should students or visitors attempt to tamper with or damage the system. The casings should also prevent the system from negatively impacting the environment around it. Since the devices are not required to be in a well lit environment, they can be kept somewhere that the sun and other weather elements would not directly affect them.

1.4 Intended Use(s) and Intended User(s)

The Challenger Learning Center has agreed to allow us to install the COSMICi project in their facility. This design project will enable the user to triangulate the point of origin of ultra high energy cosmic rays (UHECR) that enter earth's atmosphere above downtown Tallahassee, Florida. Cosmic rays most likely originate from exploding stars and a number of other cosmic events. The study of the origin of these cosmic rays is vital to understanding matter outside of this solar system. It can provide a "genetic" blueprint of the chemical composition of the universe.

The installation of this project at the Challenger Learning Center also serves as a learning experience for the upcoming young scientists of the next generation. The system will also assist astrophysicists in mapping and collecting data on different events occurring in the universe, such as merging black holes, star deaths, and other high energy occurrences. These detectors will be portable enough for individuals to set up and gather data to contribute to the global data server (MARIACHI), as well as being set up in learning centers, schools and other locations to increase the amount of global coverage and collection of data.

1.5 Assumptions and Limitations

These are the project groups' assumptions:

- The system will consist of at least 3 sensors in order to triangulate the direction of the detected ultra high-energy particles
- The sensors will share a GPS input to time-stamp the data at its relative initial detection time with a real-world time value
- The Electronic components (FPGA Boards, Power Supply, Battery, Cooling System, GPS Module, WiFi boards and Central Timing Unit) will be contained in an enclosure for safety
- A cooling system will be needed to reduce the temperature of the Stratix II chip to an ideal temperature of 0° C with a margin of ≈ +/- 2° C

- The sensors will need to be mounted in the form of an approximate equilateral triangle with 30 feet of space between each sensor
- The FPGA's high-speed components will need to operate at a frequency of 500MHz
- Reductions in memory will be made to allow for the incorporation of additional sensor inputs (at least one) and a GPS timing input
- The system will be able to take in data for 4.5 years with its new 56-bit high speed internal counter (when the board is operating at 500MHz, while at 211MHz it will operate for 10.8 years)
- A battery source using 2 NiMH batteries and a power supply (recently discovered in a usable location) will be powering components for the project.

The following are the project limitations:

- The custom FPGA board (FEDM) must have a functional frequency of 500MHz to ensure the desired ±1 ns uncertainty of each time value
- The Stratix II chip must be cooled to about 0 ºC ± 2ºC and the overall board should be about 25 °C ±5ºC (this will help the FPGA to operate at 500MHz without overheating)
- Most of the standard libraries must be kept due to their ease of use
- The mountings, if hung below the ceiling, must be high enough so that they are not a hanging hazard for pedestrians(8' elevation from floor minimum)
- The support structures need a spacing of 30 feet and must not interfere with any water sprinklers, air ducts or any other unsound structural supports
- All cables must be enclosed in a conduit to prevent hanging and exposed wires
- There is minimal funding for materials to enclose the FPGA board, therefore scrap metal from the mechanical labs may be utilized.
- Shortage of software licences for Quartus testing.

1.6 Expected End Product and Other Deliverables

- Phase I:
    - The COSMICi System will detect UHECR from at least 3 scintillator devices
    - The direction and source of the cosmic ray showers will be displayed to the user in the kiosk computer in the form of a sky map(kiosk programmed using python)
    - A power source will be configured to supply all the components
    - An enclosure will protect the circuit boards
    - A Cooling System will maintain the FPGA chip at 0 °C
    - A structural design will support the scintillator-detectors and the enclosure

- Phase II (if time permits)
    - When the project enters into Phase II there will be one FPGA board for each detector and a wireless optical synchronization clock system
    - Mirrors will be installed to direct the synchronization pulse to the receivers in each FPGA
    - Optical Timing Synchronization will be incorporated into the detector system
    - A new PCB design of the current board will be created, fixing bugs and errors on the current board and including possible ideas for an increase in memory

2. System Design – Major Components of the System

2.1 Overview of the System

figure 10 and 14 (below) shows the view of the room layout and the assembly of the parts inside the enclosure.

2.2 Major Components of the System

2.2.1 Detectors (Scintillators + Photomultiplier Tubes)

The system will have three scintillators that will be placed on the support structure. Scintillators detect and absorb the incoming radiation through Earth's atmosphere created by solar rays, supernovas, dark matter, and other uncertain origins from beyond this atmosphere. In particular, the detectors absorb energy from the high energy sub atomic particles, which are created from the decay of pions and kaons. The Photo Multiplier Tubes amplify these current pulses and transmit them to the custom board (FEDM) using coaxial cables. These detectors will be able to help triangulate the point of origin from incoming cosmic rays.

2.2.2 Front-End Digitizer Module (FEDM) custom board

The custom FPGA board (FEDM) is based on a Stratix II FPGA and is connected to the Photo Multiplier Tubes (PMT) using coaxial cables. This board handles the analog to digital conversion and contains the VHDL, Verilog and C code responsible for reading in, handling and digitizing the analog data from the detectors.

2.2.3 Wi-Fi Modules

Current Wi-Fi boards are Laird EZURiO WISDK01BI-02's. They are used to establish a wireless data connection between the boards and the central server (kiosk).

2.2.4 Central Server (Kiosk)

The central server is being written in Python and its main purpose is to receive, process and graphically display the data to the end-user.

2.2.5 Central Timing Unit (CTU)

The CTU consists of a WiFi board, the GPS sub-system, the DE3 board and the high precision oscillator.

2.2.5.1 GPS Sub-System

This consists of a GPS module that sends a serial data stream and a timing sync reference signal to the DE3 board. This acts as an absolute reference to "real world" time, rather than a relative clock cycle value.

2.2.5.2 High Precision oscillator (timing reference board)

A 10MHz signal is sent from the high-precision oscillator (timing reference board) which acts as a relative time signal that clocks a time counter which starts counting when the board begins running a data collection session.

2.2.5.3 CTU Control Software (DE3 board)

The CTU control software is being prototyped on an Altera DE3 development kit using a Stratix III FPGA. This board acts as an intermediary between the GPS, the main kiosk, and the custom FPGA board (FEDM).

2.2.6 Structural Supports

The structural support system consists of the following for each detector and enclosure: 4 I-beam clamps, 4 threaded rods, and a wooden platform. Each of the threaded rods will have one of their ends bolted to a corner of the platform. The other end will be bolted to a clamp which will be fastened to a side of the I-beam.

2.2.7 Enclosure

The enclosure will be constructed from a birch plywood ¾" plate with a clear plastic cover over the base plate and circuitry, power supply, and cooling system. An acrylic Plexi-Glass® sheet will be hinged on top of the clear plastic cover allowing easy viewing of the inside components. It will have a key lock so that the contents are protected, and still easy to access. This will be

mounted upside down with the base connected to the structure and the Plexi-Glass® door facing down for users to view.

8.

2.2.8 Cooling System

The cooling system consists of a copper rod, a peltier cooler, copper heat sink fins, and a fan to remove heat from the system. Heat generated by the FEDM chip will travel through the copper heat pipe to the peltier cooler which will create the heat dispersal through the fins and fan. The cooling systems main task will be cooling the FPGA chip so that it can operate at its maximum frequency.

2.2.9 Power Supply

All components are currently being powered by outlets and an adjustable power supply in the lab. Since the goal is to have these installed in the Challenger Learning Center, we need an alternative solution for powering every component.

There is a suitable power supply in the lab that we will use to provide power for the FEDM, CTU, and two of the Detectors. The third detector will be battery powered.

2.3 Performance Assessment

2.3.1 Structural Support

The newsupport system design will have one detector and the circuit board enclosure safely suspended from the ceiling. The additional two detectors will be housed on a shelving unit currently being designed will be ≈ 30’ apart. The center’s safety representative requested that all hanging equipment be attached to the building structure i.e. I-beams. The structural support design meets the requested safety guidelines as well as the load requirements above and beyond the required safety factor. Each scintillator weighs 25 lbs and the corresponding set of beam clamps supporting the detector has a combined capacity of 2000 lbs (4 X 500lbs).

2.3.2 Power Supply

Each component of the project has to be supplied by a certain amount of power. Power for the CTU, the FEDM, and two of the detectors will be provided by a 250W power supply. This power supply provides voltages of 12V, -12V, 5V, 3.3V, and GND (0V). All voltages for each component of the project can be supported. The total power drawn by the components is well under 250W so this power supply holds more than enough power for each component.

The third detector will be battery powered by a 12V, 4.5Ah Li-ion rechargeable battery. This detector will be used for demonstration purposes. The detector requires a current of 21mA with 12V so this battery is definitely suitable to provide power for ≈ 2.5 weeks before needing to be charged (refer to appendix for detailed calculations).

2.3.3 Enclosure

The enclosure will house all the PCB's, the power supply, and the cooling system. It will protect them from physical shock and foreign object debris. Also it will be hung from the ceiling with a clear cover so that all components are easily viewable for the public. The enclosure will have vents to support the airflow throughout the system allowing excess heat to dissipate. The cooling system will be mounted inside the enclosure with the heat pipe and peltier cooler attached directly onto the board. The whole system will be hung from the ceiling by a structural support. The clear cover will be hinged and keyed for secured access to the boards and power supplies in order to make changes, while keeping unwanted personnel out.

2.3.4 Cooling System

The cooling system design will provide greater than three times the heat removal from the Stratix II chip. Using copper instead of the current aluminum block, the thermal conductivity will increase from 120 W/m*K to 398 W/m*K. This will create a heat transfer rate of 70 W. Also using copper heat fins, the fan will dissipate the heat from the system at higher rate as well.

2.3.5 Bit-Width Reduction

In order to add an additional sensor input and time-stamping input from the GPS, the FPGA board will have some of its memory freed up. To free up this memory the word size used in the FIFO and Pulse-Path components was reduced from 64 to 56 bits. This freed up the space needed for additional inputs. There was enough room to add an additional sensor input data path, and begin implementing the GPS timing sync input path to time-stamp the data.
These were the results of the freed space as of November 3rd, 2011:

Before:

- Slow corner fmax for high-speed counter: 211.28 MHz
- Logic utilization: 24,314/27,104 (90%) = 2,790 remaining
- Dedicated logic registers used: 21,878/27,104 (81%) = 5,226 remaining
- M512 blocks: 193/202 (96%) = 9 remaining
- M4K blocks: 144/144 (100%) = 0 remaining
- M-RAM blocks: 1/1 (100%) = 0 remaining

After:

- Slow corner fmax for high-speed counter: 213.13 MHz (only slightly better)
- Logic utilization: 22,007/27,104 (81%) = 5,097 remaining (almost 2x as much left)
- Dedicated logic registers used: 19,463/27,104 (67%) = 7,641 remaining (about 25% better)
- M512 blocks: 188/202 (93%) = 24 remaining (more than 2x better)
- M4K blocks: 144/144 (100%) = 0 remaining (same as before)
- M-RAM blocks: 1/1 (100%) = 0 remaining (same as before)

-From Dr. Frank's blog at http://cosmicinquirer.blogspot.com/

2.3.6 FPGA Operational Frequency Increase

All high-speed components of the Front-End Digitizer Module (FEDM) will be logically optimized using Quartus' Logic Locking feature. This will be utilized to bring the FPGA board back from its current 200MHz operational frequency to the prior 500MHz. Using logic lock will prevent Quartus from "optimizing" the logic elements in the way it sees fit and keep the designers exact specifications in order to reduce the amount of memory usage. All of the circuit components that use the Pulse-Locked Loop will have to be logic locked. This is also a part of the projects goal to free up memory on the board for additional inputs. The high speed counter module, pulse cap modules and time sync module use the PLL and will be logic locked. This task has not yet been worked on but has been planned out.

2.3.7 FEDM Firmware Changes

Two new parallel inputs/outputs (PIOs) will be added to the System on Programmable Chip design (one for a new timing sync data path and for its control register). Then, a new firmware driver will be written in C to control the new PIOs. The firmware has been modified to utilize the new time data.

2.3.8 The Input Capture/ Timing Sync Datapath (ICDP) for the FEDM

A new version of the ICDP is being created to disregard the voltage thresholds 2-6. It is now only concerned with the first voltage threshold. This module will only be triggered by the rising edge of the threshold.

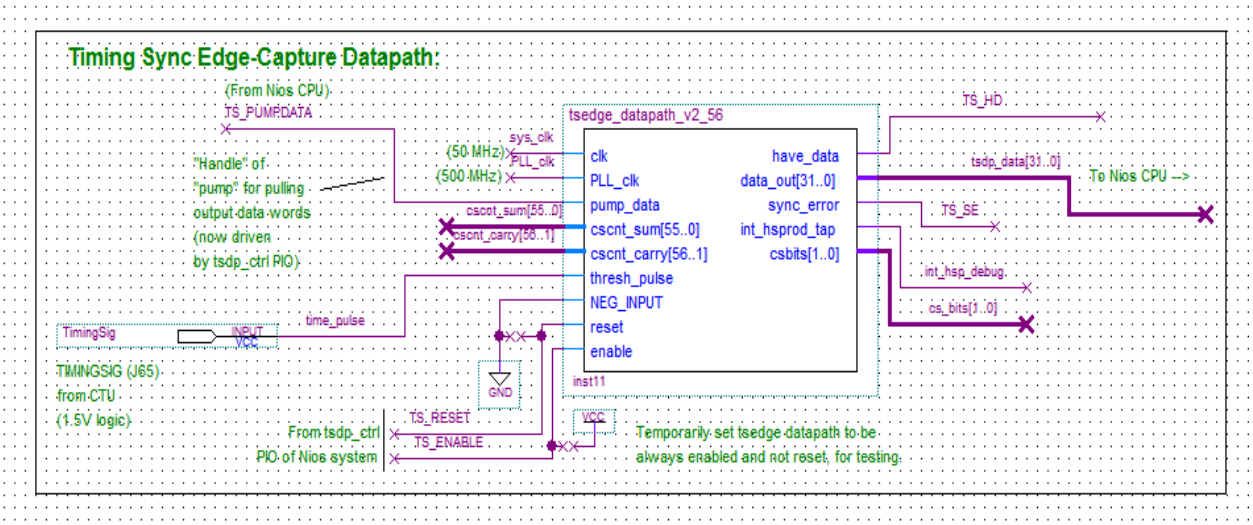


Figure 1- Timing Sync Datapath block

2.4 Design Process

2.4.1 Structural Support

The current structural design will be modified. The new design will have the enclosure and one scintillator suspended below the drop ceiling and have the other two suspended on shelves. Furthermore, the client expressed the desire for the detectors to be spread across the 2 adjacent classrooms at the CLC. The support system will not block or interfere with any sprinklers or air ducts. Also one of the scintillator-detector supports will be slightly modified to accommodate two batteries that will power that detector.

2.4.2 Enclosure

The enclosure design is finalized and all components fit perfectly inside. The circuit boards were measured and drawn in ProE to establish a visual model of the layout and enclosure of all the components (image shown later). The system will be sized and a physical layout will be tested in order to ensure that all components can connect to each other.

2.4.3 Cooling System

The cooling system design began with the current implemented system. Due to budget and time constraints, the peltier cooler is the ideal method to continue the cooling of the Stratix II chip. Modifications to the heat pipe and heat sink apparatus will allow for the device to remove ≈ 70W of heat from the chip; more than enough to cool it to 0ºC.

Cooling System Design Decision Matrix

Method	Peltier Cooler	Liquid Cooling	Convection Heat Sink
Cost	4	3	5
Effectiveness	4	5	1
Design Level	4	3	4
Time Frame	5	4	5
Safety	5	4	5
Total	22	19	20

Score 1 to 5, 5 being the best

2.4.4 Power Supply

Using a proto board to distribute the voltages is the best decision for powering the CTU, FEDM, and the two detectors (Refer to Appendix).

For the battery powered detector, we will use two Li-ion rechargeable batteries and connect them in parallel. We will need a connector for the batteries and proper connections to insert them into the detector.

2.4.5 Bit-Width Reduction

To effectively reduce the bit width, generic values were defined for use in the files "h_speed_counter", "fifo_reader", "fifo_writer", "cs_combine", "se_pulse-cap" and "stream_pulse_data" so that future size changes to the bit width will be simple to implement. Once the code for the VHDL and Verilog components was edited they were recompiled and renamed with "_56" tags. Next the code was recreated into block diagrams from the lowest level, where they were then re-implemented up to the top-level of the block diagrams. Once this was completed it was given to Dr. Frank to insert into the current top level diagram. After some debugging the code was added to the project and freed up more memory allowing for implementing additional inputs.

2.4.6 FPGA Operational Frequency Increase

All high-speed components of the Front-End Digitizer Module (FEDM) will be logically optimized using Quartus' Logic Locking feature. This will be utilized to help bring the FEDM chip back from its current 211 MHz operational frequency to the prior 500 MHz. Logic Lock will prevent Quartus from automatically optimizing the logic elements in the design. All of the circuit components that use the Phase-Locked Loop (PLL) will have to be logic locked. This will reduce the amount of logic elements in the design which will increase the operational frequency.

2.4.7 FEDM Software

A new input timing sync path - parallel input/output (PIO) - will be added to the System on the Programmable Chip (SoPC) design and a new firmware driver will be written in C. Code has been written that will associate the timing data to the pulse data.

3. Design of Major Components

3.1 Bit-Width Reduction

In order to free up space on the DE3 board for additional inputs the current bit-width of the recorded voltage pulses was reduced. This consisted of reducing the bit width of several components from 64 bits to 56 bits in width. Once the width was reduced, the block diagrams were relabeled. Afterwards, the new block diagrams of the VHDL and Verilog code files were incorporated into the main design file and tested for errors.

Images of reduced block diagrams before and after (just a few for example purposes)

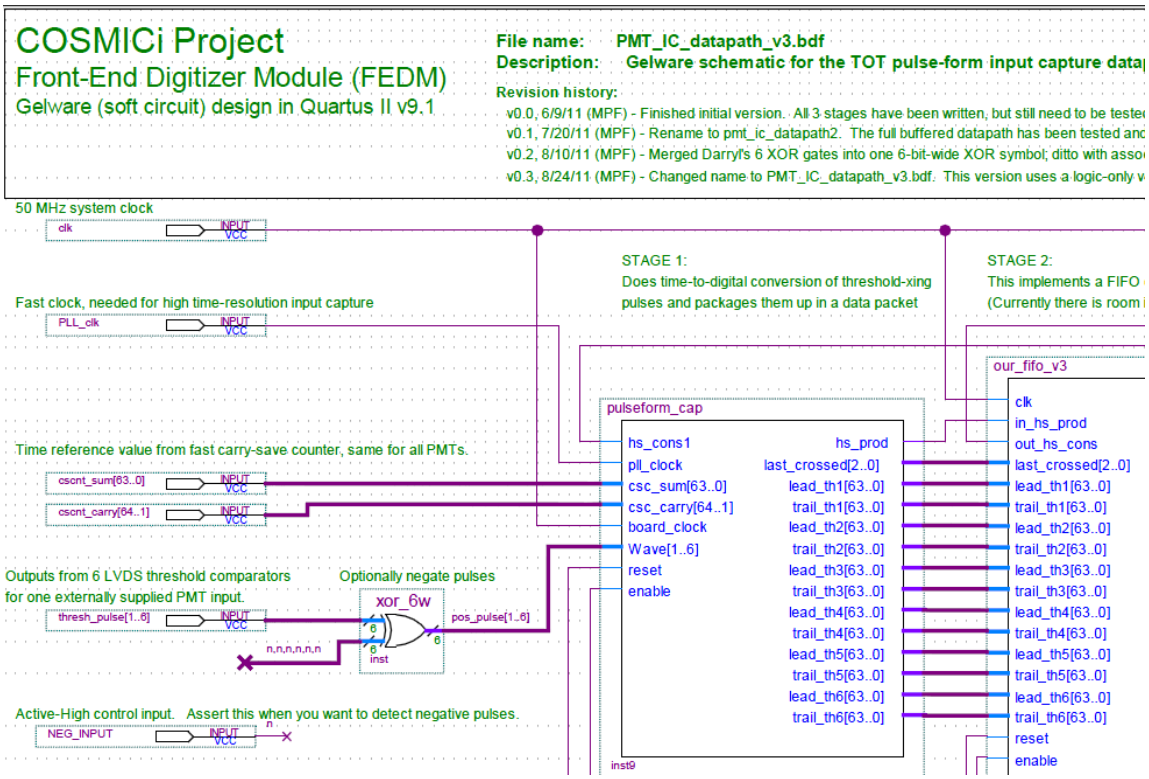


Figure 2- Image of the block diagram before the bit reduction

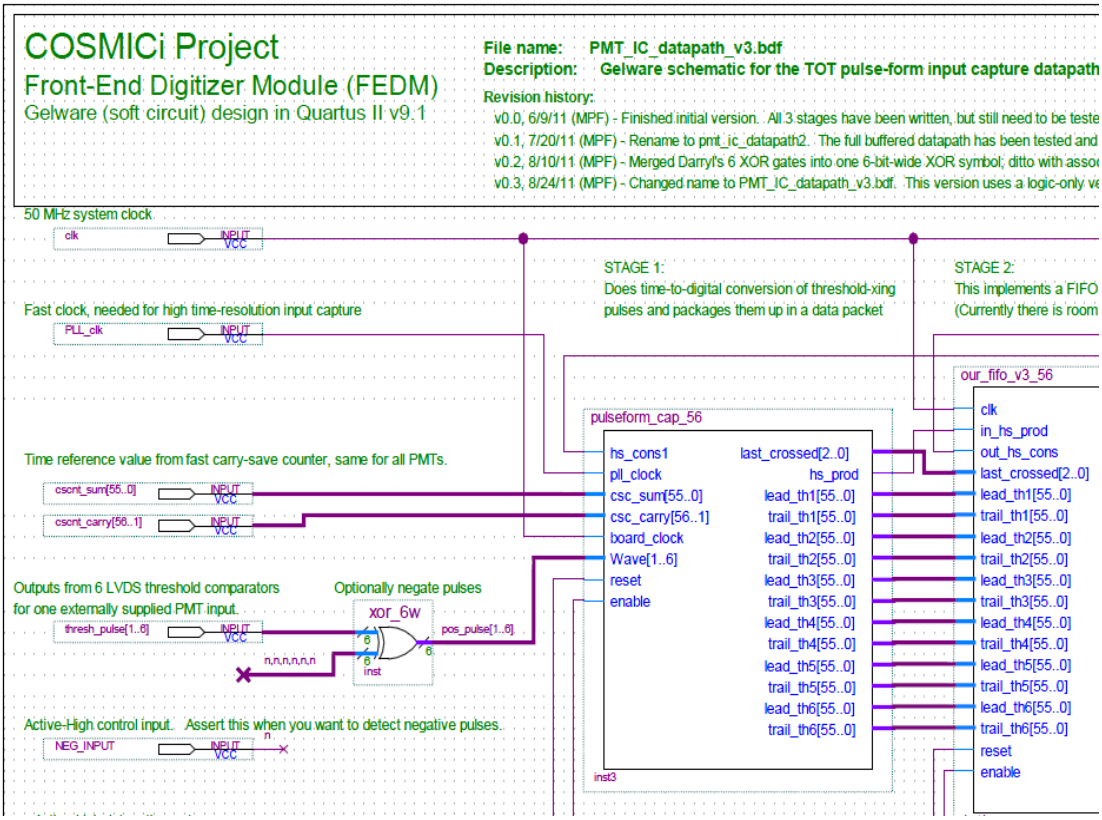


Figure 3- Image of the same block diagram after the bit reduction

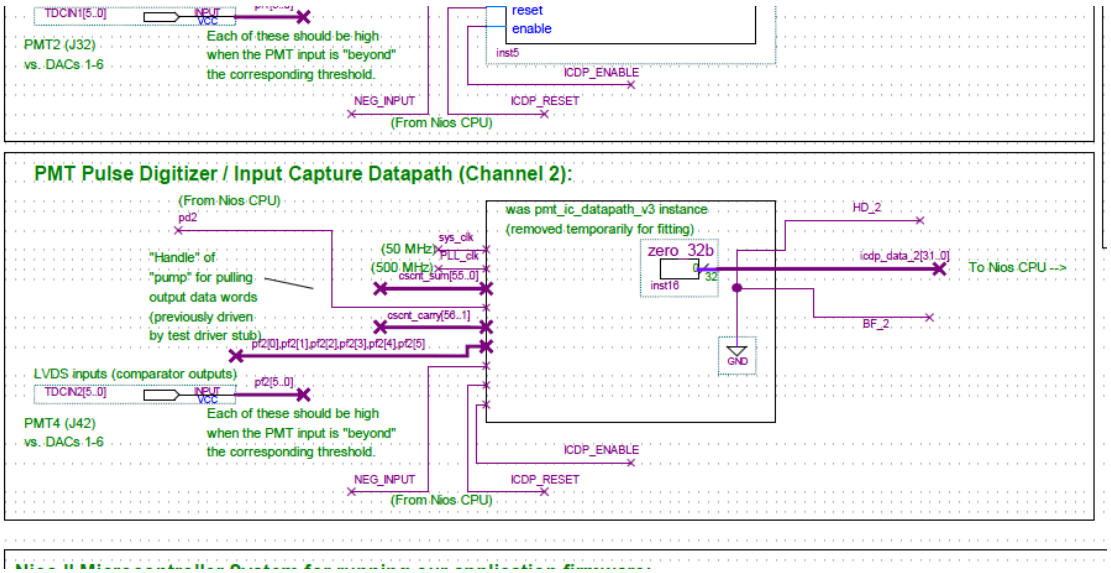


Figure 4- Image of the Top level diagram before the third input could be incorporated

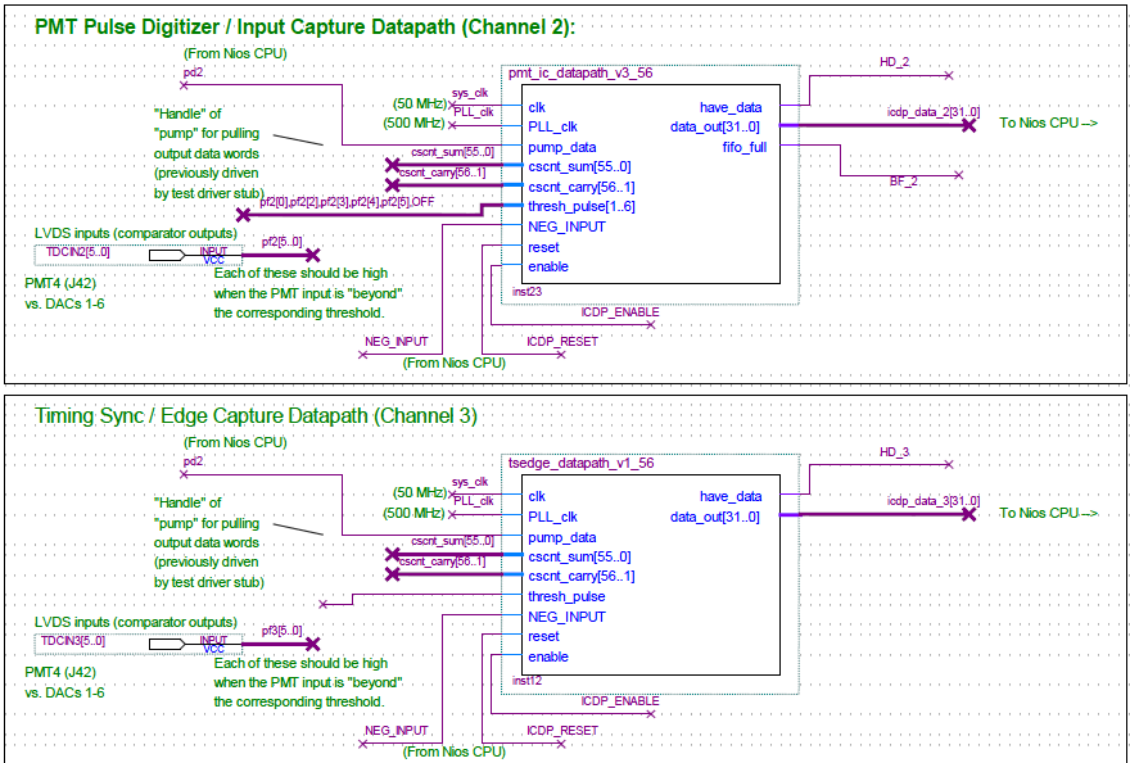


Figure 5- Image with the third input added to the design

3.2 Logic Locking of High Speed Components

This section of the project will consist of speeding up the FPGA's operational frequency to its initial 500MHz. Currently it is operating at 211MHz and does not produce the required precision of 2 ns between each data reading.
The Quartus Logic Locking feature will be utilized to ensure that the components operate at 500MHz by not allowing Quartus to optimize the logic elements. The automatic optimization feature slows down the clock.

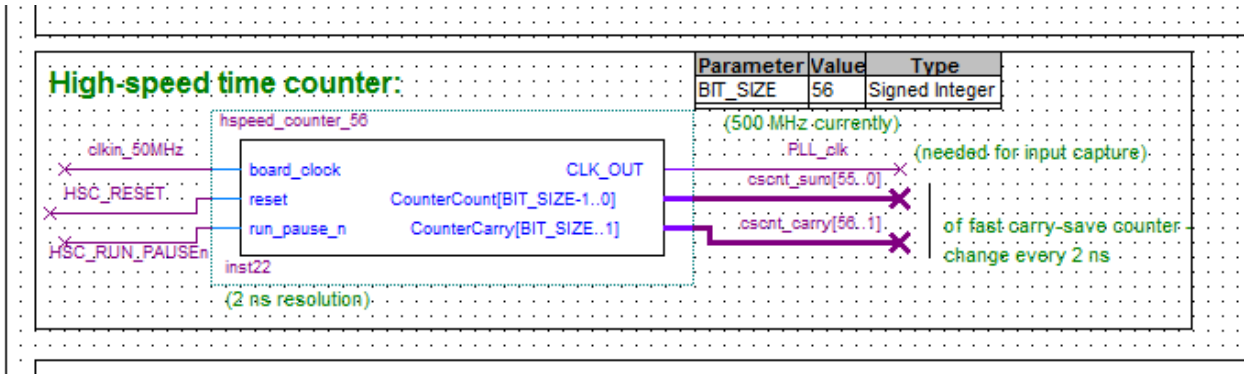


Figure 6- Shows Initial PLL clock line

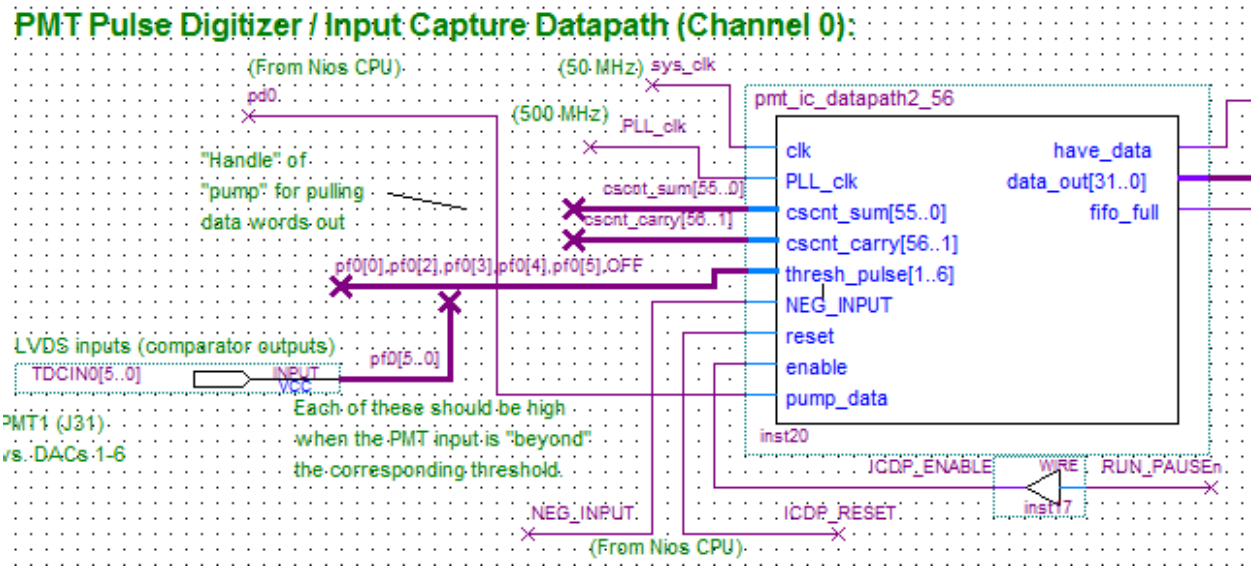


Figure 7 – Top Level PMT Input Capture Datapath Using PLL Line

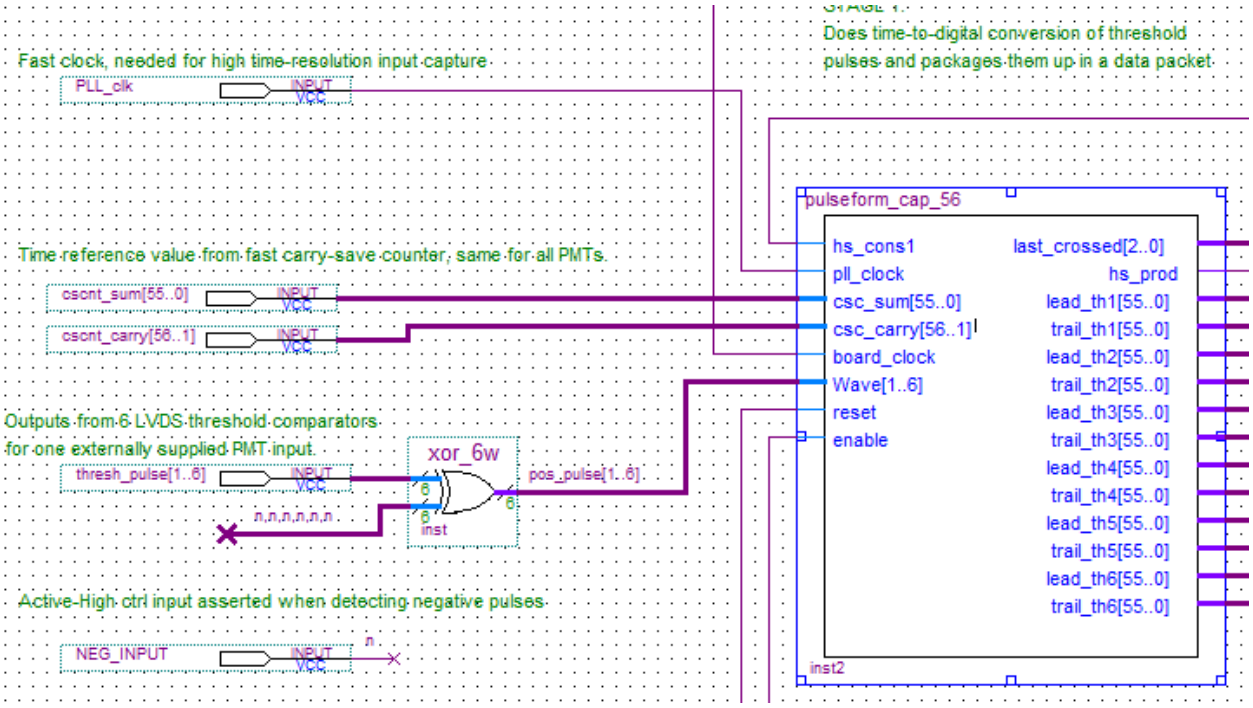


Figure 8 – Individual PMT Datapath Using PLL Line

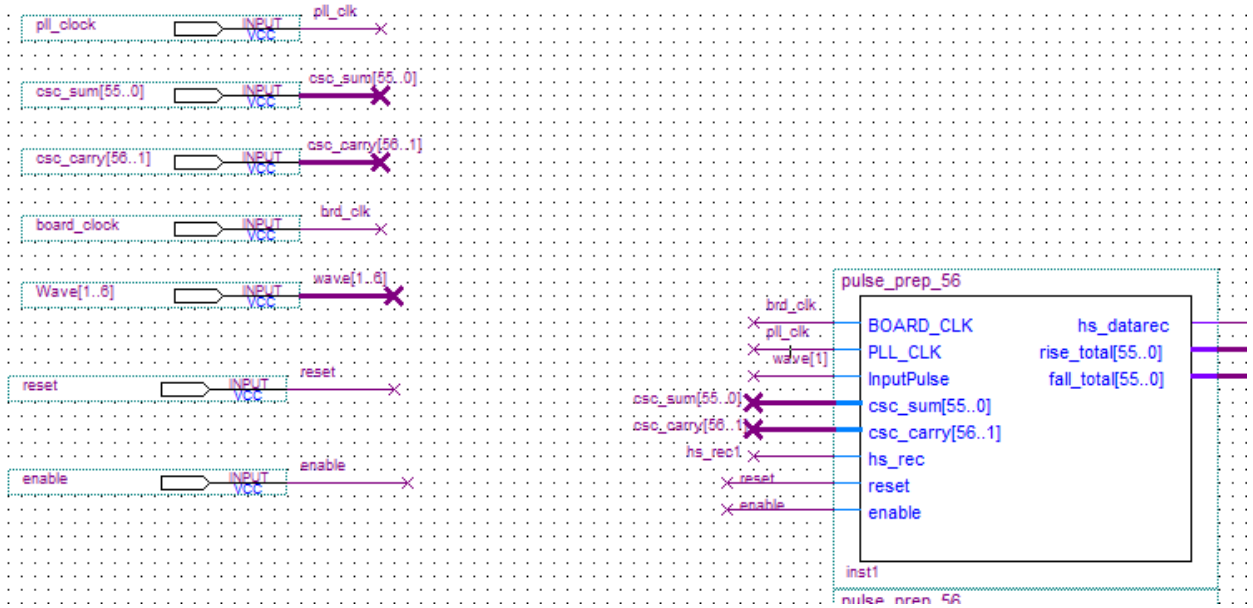


Figure 9 - Pulse Cap using the PLL Line

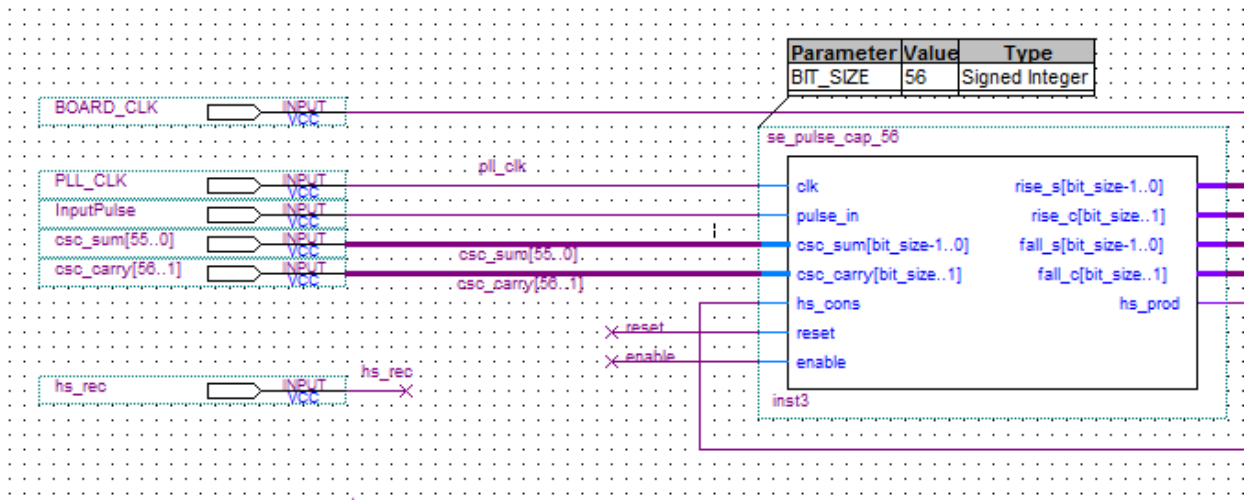
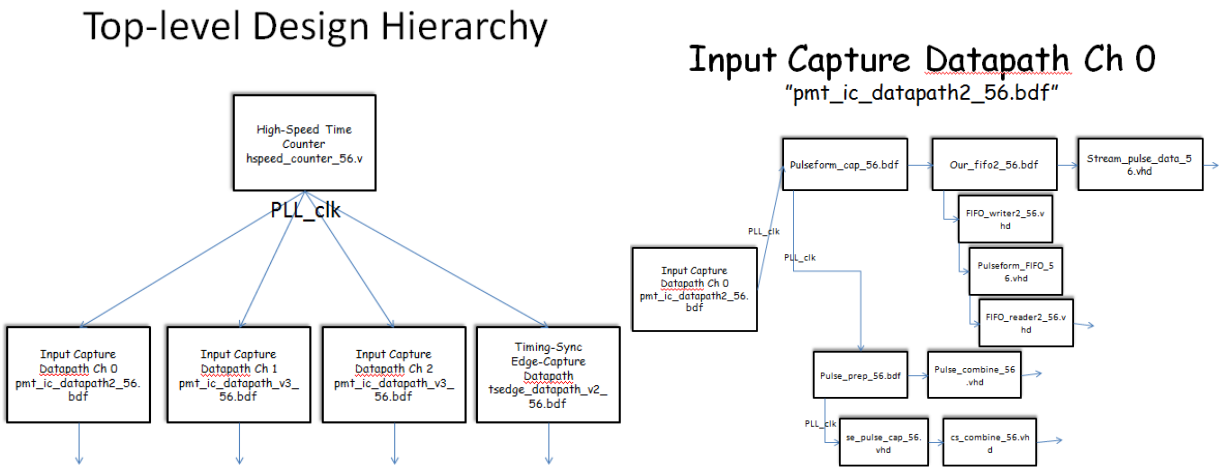
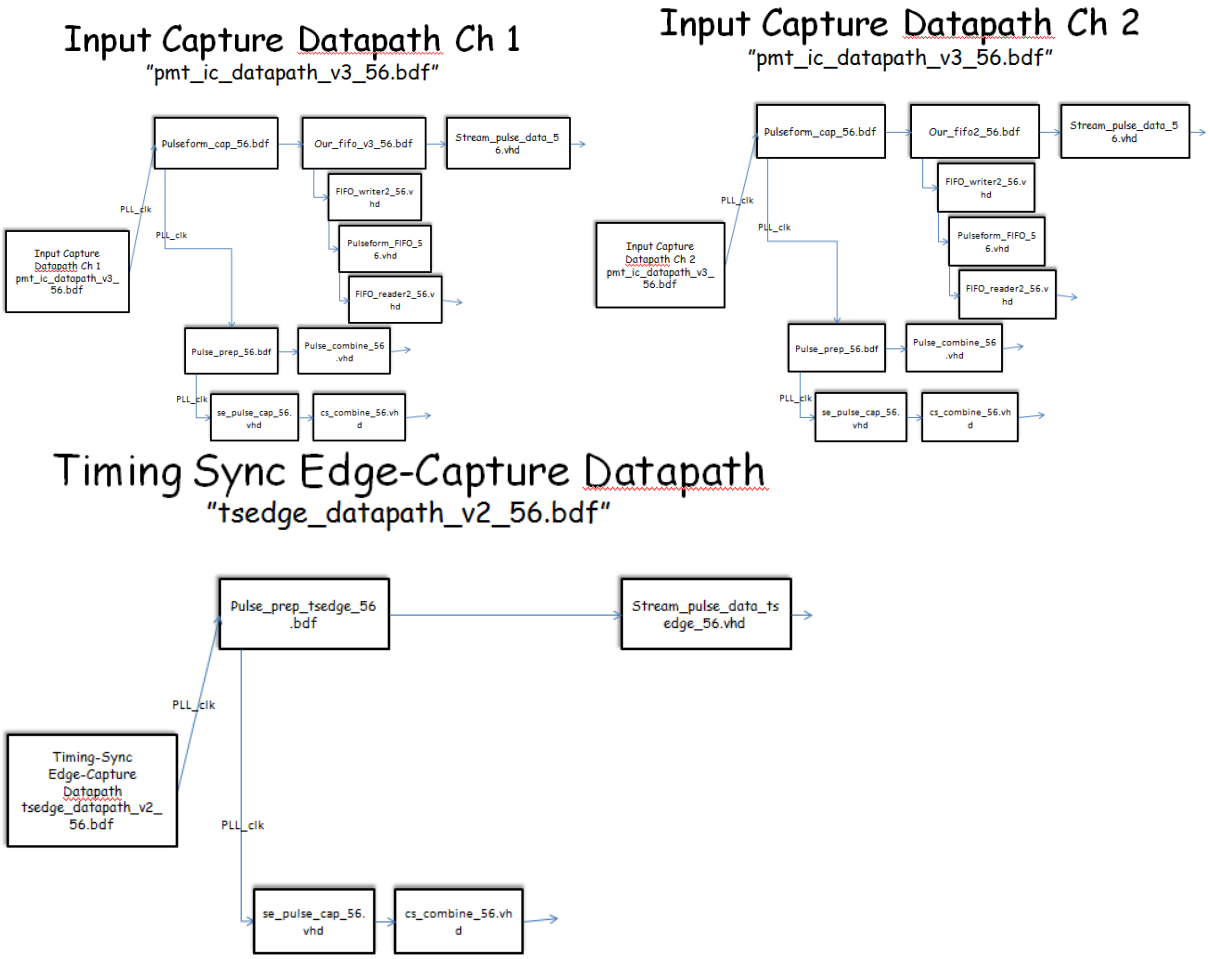


Figure 10 - Pulse Prep using PLL Line

The components that utilize the PLL_clock are the ones that require logic locking to speed up the high-speed clock. Below is a diagram showing the different components that directly utilize this clock line.





The lines that have the PLL_clk labeled will be placed into the LogicLock regions and connected to the top level root region in Quartus.
The blocks that will be Logic Locked are:

At Top Level:
- Input Capture Datapath Ch0
- Input Capture Datapath Ch1
- Input Capture Datapath Ch2
- Timing Sync Datapath

Inside Ch0:
- Pulse Form Cap
- Pulse Prep
- SE Pulse Cap

Inside Ch1:
- Pulse Form Cap
- Pulse Prep
- SE Pulse Cap

Inside Ch2:
- Pulse Form Cap
- Pulse Prep

SE Pulse Cap
Inside Timing Sync
Pulse Prep TSEdge
SE Pulse Prep

3.3 Power Supply

3.3.1 FEDM, CTU, Two detectors

The power for the FEDM, CTU, and two Detectors will be provided by a 250W power supply. The power supply will be connected to the 24 pin header of the PCB. Connections from the header to the desired location on the power distribution board will distribute the voltage for the different components of the project. The power distribution board will be created using PADS PCB software. (Refer To Appendix)

3.3.2 Detector

The third detector will be battery powered and used for demonstration of portability. The detector requires 12V at 21mA. The battery that will power this detector will be a Li-ion 12V, 4.5Ah battery. Having two of these batteries connected in parallel will result in a 12V, 9Ah battery. A battery with these values would last ≈ 2.5 weeks (based on the measured values of the detector). To make this connection we will need a connector to connect both the positive terminals of the battery and the negative terminals of the battery. We will then need extra connectors that can be soldered to a barrel plug. When this connection is complete, the barrel plug will be placed into the detector to provide the power.

3.4 Structural Support

3.4.1 Wall Support Shelf Design

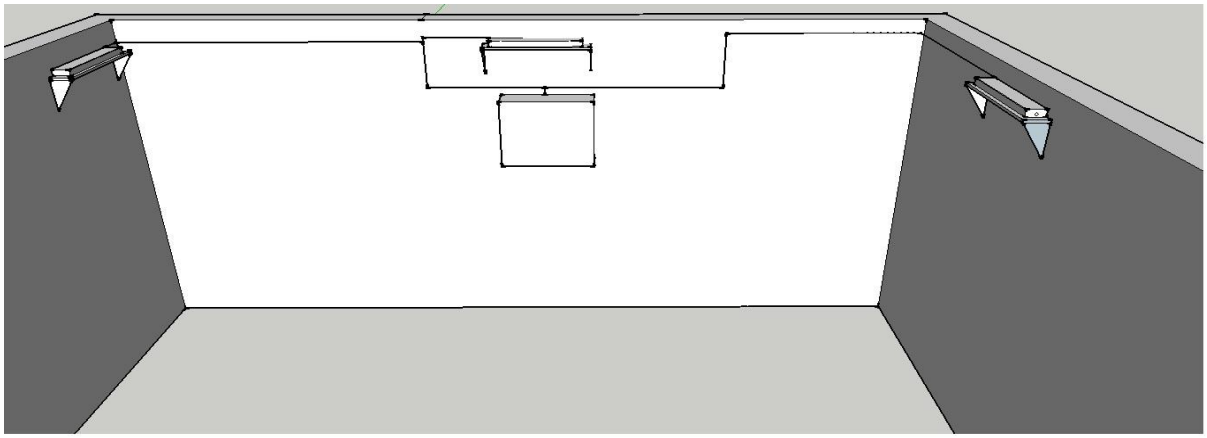


Figure 10 – Wall support design

Description

In this configuration, two network elements are supported by structures attached to the walls. Each element will be supported by a shelf. The shelf will be supported by a heavy duty bracket attached to structural stud's in the wall.

3.4.2 Suspended Detector Design

The current design consists of 3 scintillator-detectors forming a triangular configuration and a circuit board enclosure. This suspended detector will be hanging from I-beams in room 119 at the Challenger Learning Center to form an equilateral triangle configuration. Each side of the triangle must be 30 ft long with a tolerance of 2 to 3 ft. One of the detector support platforms will also support two 2.2 lbs batteries (4.4 lbs total).

Figure 11 – Scintillator Guncase Support Dimensions

3.5 Enclosure

The ideal material selection for the clear plastic cover is plastic Plexi-glass®, and the base will be made from birch plywood. The cover will be attached using several hinges on one side and a keyed lock on the other for easy, yet secure entry and access to the enclosed components. The system will be hung upside down allowing for easy viewing of working components. Some additional lights could be added for extra aesthetic effect.

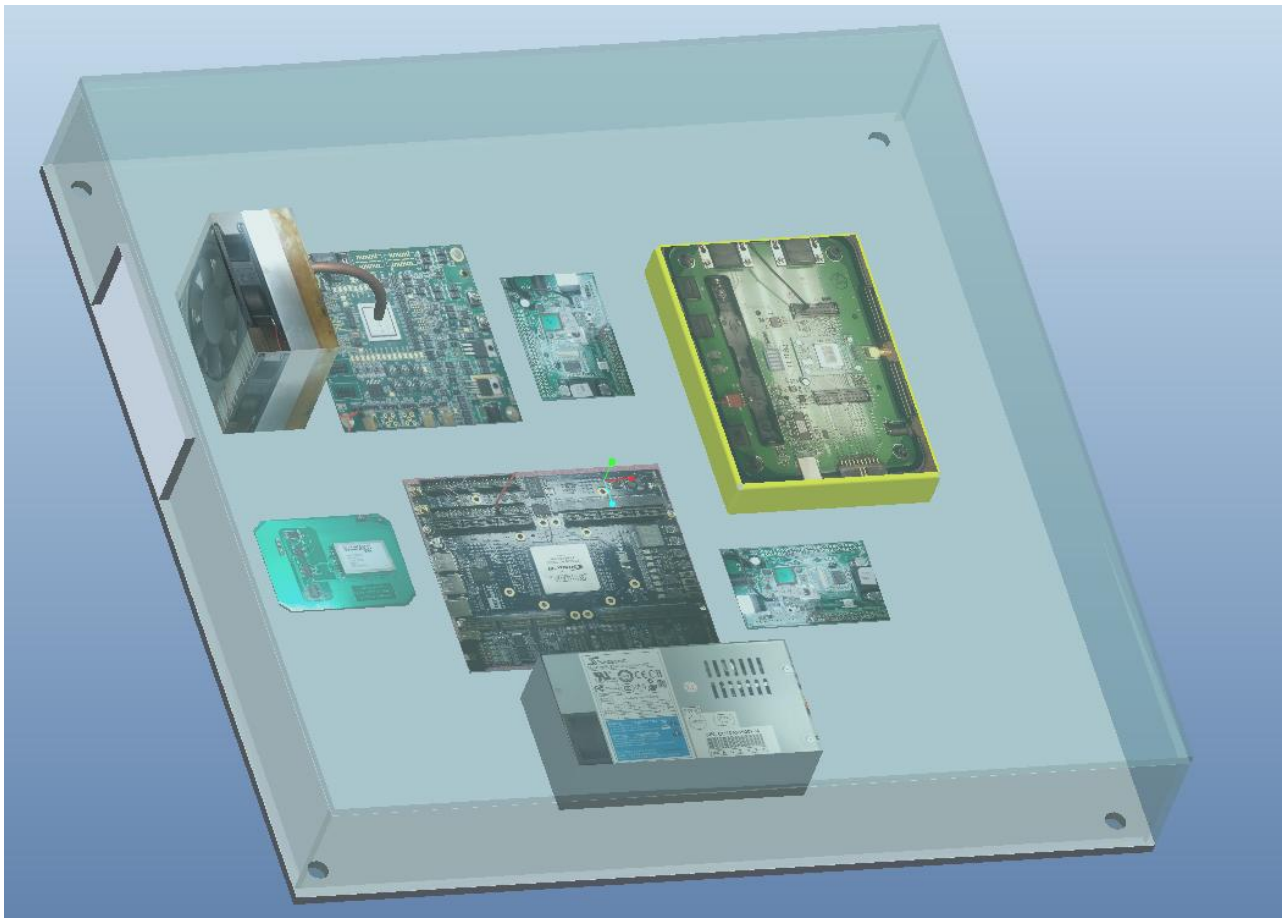


Figure 12 – Enclosure Component Layout and Cooling System

3.6 Cooling System

The final designed cooling system will include some of the initial design components (the Peltier Cooler and fan) along with added materials to decrease the temperature of the chip and the surrounding voltage regulators. The aluminum block will be replaced with a solid copper heat pipe due to its higher thermal conductivity of 398 W/m*K compared to Aluminum's 120 W/m*K. The current operating temperature is 8°C. With the newly added copper fins and heat pipe, along with a new peltier cooler and fan, a higher heat transfer rate will remove heat faster from the chip creating a lower operating temperature.

Although using copper will increase the heat rate transfer from the Stratix II chip, it will still create condensation build up on the copper pipe as it does on the current aluminum block. To solve this problem, the pipe will be coated with a spray foam polyurethane insulation. This will eliminate condensation forming on the pipe and chip, thus solving the current issue of water damage to the chip and board.

All needed materials have been purchased and are awaiting delivery. The copper rod and heat sink assembly are scheduled to arrive Feb. 7. The new thermoelectric coolers will not arrive

until Feb 28th. Therefor,e for testing purposes, the current thermoelectric cooler will be used until arrival.

4. Test Plan

4.1System and Integration Test Plan

The project consists of two major tests of the major components when that are connected together to form a functioning unit as well as minor tests on each component. There will be a major test for the for the major ECE components to be sure that the components are functioning properly and giving correct/anticipated results. After the test on the ECE major component has been performed, a test on the ME components will be tested since they depend on the ECE components.

4.2Test Plan for Major Components

4.2.1 ECE Components

4.2.1.1 Power Supply/Batteries

Testing Sheet

Test Item: Power Distribution Board
Tester Name: Samad Nurideen
Tester ID No:xxxxxx893
Test Date: 02/15/12
Test No: 1
Test Time: 3:00PM
Test Type: Test
Test Location: Frederick Humphries Building
Test Result: TBD

Test Objective:
The objective of this test is to make sure the power supply distributes the desired voltages to the different components of the project

Test Description/Requirements:
The equipment required for this test will be:

- Power Supply
- Power Distribution Board
- FEDM
- CTU

Anticipated Results: The FEDM and CTU function correctly at the same time

Requirement for Success:
No lag in currents for both components

Actual Results:
TBD
Reason for Failure:
N/A

Recommended Fix:
N/A

Other Comments:

Testing Sheet

Test Item: Lithium Ion Rechargeable Battery Pack
Tester Name: Samad Nurideen
Tester ID No:xxxxxx893
Test Date: 02/29/12
Test No: 1
Test Time: 3:00PM
Test Type: Test
Test Location: Frederick Humphries Building
Test Result: TBD

Test Objective:
The objective of this test is to see if the battery has the correct voltage and current needed to power the detector.
In addition, the test will determine if the selected battery will last as long as predicted.

Test Description/Requirements:
The equipment required for this test will be:

- Voltmeter
- Ammeter
- Battery
- Alligator Clips
- Connectors
- Detector

Anticipated Results: The battery when connected in parallel has the correct voltage and current. And does not stop powering the detector until 2 weeks later

Requirement for Success:
Detector functions properly while being powered by the battery

Actual Results:
TBD
Reason for Failure:
N/A

Recommended Fix:
N/A

Other Comments:

4.2.1.2 Logic Lock Frequency Testing

The frequency that the board is operating at can be obtained in the compilation report. This gives a simulated operational frequency. There is also a timing analysis tool that can be utilized in the Quartus tools tab. After placing the blocks utilizing the PLL_clock line into the Logic Lock regions the design will them be compiled and run through the **Classic Timing Analyzer Tool** to see the calculated frequency. Once the reading on Quartus is around what is desired it can be tested in actual run time while collecting input test data.

Testing Sheet

Test Item: Operational Frequency
Tester Name: TBA
Tester ID No:
Test Date: TBA
Test No: 1
Test Time: 2:30PM – 5:00PM
Test Type: Test
Test Location: Frederick Humphries Building
Test Result:

Test Objective:
The objective of this test is to test for any increase in the operational frequency.

Test Description/Requirements:
The equipment required for this test will be all of the ECE system components Including:

- FEDM, CTU
- DE3 board
- Power Supply
- Quartus Software and License

Anticipated Results:

Requirement for Success:
Able to operate the board at a frequency of 500MHz or higher.

Actual Results:

TBD

Reason for Failure:
N/A

Recommended Fix:
N/A

Other Comments:

4.2.1.3 Input Capture and Timing Sync Datapaths

The input capture datapaths and timing sync datapaths will be tested to determine if they are functioning properly. Both datapaths depend on signals from PMT/scintillator arrangements. The information obtained from the datapaths will be checked and the timing stamp from each datapath will also be checked and compared.

Testing Sheet

Test Item: Datapaths
Tester Name: TBA
Test Date: TBA
Test Time: 2:30PM
Test Location: Frederick Humphries Building
Tester ID No:
Test No: 1
Test Type: Test
Test Result:

Test Objective:
The objective of this test is to verify which that the input capture datapath and the timing sync datapath are functional

Test Description/Requirements:
The equipment required for this test will be all of the ECE system components Including:

- Scintillator detectors/PMTs
- FEDM, CTU
- DE3 board
- Power Supply
-

Anticipated Results:

Requirement for Success:
Able to configure sufficient pins of the PIC18F8722 can be configured and used as outputs.

Actual Results:
TBD

Reason for Failure:
N/A

Recommended Fix:
N/A

Other Comments:

4.3ME Components

4.3.1.1 Structural Support

The structural supports must be tested to ensure they perform as expected.

Testing Sheet

Test Item: Structural Supports
Tester Name: Brian Kirkland — Tester ID No:
Test Date: TBA — Test No: 1
Test Time: TBA — Test Type: Test
Test Location: TBA — Test Result:

Test Objective:
The objective of this test is to verify that the structural supports can hold the specified weights and allow a factor of safty as well. This test will show that the clamps, rods. bolts, nuts, and shelving units will not fail under a perscribed amount of stress.

Test Description/Requirements:
The equipment required for this test will be::

- Supports
- Weights
- Force Gague

Anticipated Results: The supports can hold well over the perscribed ammount of weight and as such will perform as expected/needed withouth damaging them by testing with the actuall loading size.

Requirement for Success:

No failure/extremely limited deflection
Actual Results:
TBD
Reason for Failure:
N/A

Recommended Fix:
N/A

Other Comments:

4.3.1.2 Cooling System

Due to material delivery status, all new components will be tested to ensure optimal operating temperature will be achieved. Current thermoelectric cooler will be used for testing purposes until arrival of new thermoelectric coolers in late February.

Testing Sheet

Test Item: Cooling System
Tester Name: George Chakhtoura
Tester ID No:
Test Date: 02/13/12
Test No: 1
Test Time: 3:00PM
Test Type: Test
Test Location: Frederick Humphries Building
Test Result: TBD

Test Objective:
The objective of this test is to assemble and obtain temperature readings using new heat transfer rod and heat sink assembly.

Test Description/Requirements:
The equipment required for this test will be:

- Straight Polyurethane Coated Copper Rod
- Copper Heat Sink Assembly
- Current Thermoelectric Cooler

Anticipated Results: The temperature of the Stratix II chip will reach approximatly 1^{o} C with minimal condensation build up on heat transfer rod.

Requirement for Success:
Chip temperature reaches 0^{o} C.
Zero condensation build up on rod.

Actual Results:
TBD
Reason for Failure:

N/A

Recommended Fix:
N/A

Other Comments:

4.3.1.3 Enclosure

The enclosure must be tested to make sure it will operate as designed. Testing will ensure no unforeseen flaws exist in the system which could lead to failure of the device.

Testing Sheet

Test Item: Enclosure
Tester Name: Brian Kirkland
Tester ID No:
Test Date: TBA
Test No: 1
Test Time: 2:30PM
Test Type: Test
Test Location: TBA
Test Result:

Test Objective:
The objective of this test is to verify which that the enclosure will hold all the weight prescribed and a factor of safety to make sure the baseplate does not deflect too much or crack under stress.

Test Description/Requirements:
The equipment required for this test will be:

- Baseplate
- Weights
- Holding apparatus

Anticipated Results: The baseplate can hold well over the prescribed amount of weight and as such will perform as expected/needed

Requirement for Success:
No failure/extremely limited deflection

Actual Results:
TBD
Reason for Failure:
N/A

Recommended Fix:
N/A

Other Comments:

5. Percentage Completion

5.3 Power Supply and Batteries

Power Supply – 80% of Overall Task Goal

Subtasks:

Power FEDM – 10%	Complete	10/5/11
Power CTU – 10%	Complete	10/19/11
Power both CTU and FEDM – 70%	40%	
Provide Power for detectors – 10%	40%	

42 % OF POWER SUPPLY GOAL IS COMPLETE

Battery – 20% of Overall Task Goal

Subtasks:

Research – 30 %	Complete	10/20/11
Order Parts – 10%	0%	
Implement – 40%	0%	
Test – 40%	0%	

30 % OF BATTERY GOAL IS COMPLETE

40% OF POWER SUPPLY/BATTERY GOAL COMPLETE

5.4 Cooling System

Subtasks:

Temperature Measurements of Chip and Board –5%	Complete	11/7/11
Physical Measurements of all Boards – 5%	Complete	10/20/11
Peltier cooler, fins, and fan cad design – 15%	Complete	11/8/11
Solve Condensation Issue –10%	Complete	11/8/11
Provide heat equations showing chip temp – 30%	Complete	02/01/2012
Order correct size peltier cooler, fins and fan –5%	Complete	02/01/2012
Connect cooling system to structure–5%	0%	
Test for Issues–25%	0%	

70 % COOLING SYSTEM GOAL IS COMPLETE

5.3 Timing Sync Data Path

- Research system level design (11/5 - 11/18) ----- Complete
- Implement design (11/21 - 12/9) Complete
- Testing (12/9 - 1/12)

5.4 Central Server Visualization Feature

- Research Google Earth API (1/9 - 1/20)
- Implement design (1/23 - 2/10)
- Testing (2/10 - 2/19)

5.5 Code Reduction/Add Datapath

Code Reduction – 80% of Overall Task Goal

Subtasks:

• Familiarize with Code – 5%	Complete	9/21/11
• Implement Global Variables–30%	Complete	10/5/11
• Recreate Newly Sized Component Blocks – 30%	Complete	10/19/11
• Re-wire and Re-label Components – 10%	Complete	10/23/11
• Debug and Test for Completion – 5%	Complete	11/2/11

100 % OF CODE REDUCTION GOAL IS COMPLETE

Add Additional Input – 20% of Overall Task Goal

Subtasks:

Add additional Input VHDL Code – 10 %	Complete	11/2/11
Test for Errors – 10%	Complete	11/2/11

100 % OF ADDITIONAL INPUT IS COMPLETE

100 % OF CODE REDUCTION/DATAPATH GOAL COMPLETE

5.6 Logic Locking High Frequency Components

This portion of the goal has not been started as of yet**.** There are pending steps that must be completed before it can be worked on.

Subtasks:

- Research Logic Locking – 5% TBD
- Logic Lock Lowest Level Components – 25% TBD
- Test Frequency Operation Level – 10% TBD
- Logic Lock Additional Levels – 25% TBD
- Test Frequency Operation Level – 10% TBD

Subtasks:

- Test Integration of New Frequency – 15% TBD
- Test For Errors – 10% TBD

0 % OF OVERALL LOGIC LOCKING GOAL COMPLETE

5.7 Enclosure

Subtasks:

- **Base plate:** 45% 45%
  - Designing : 31.5%
  - Machining: 13.5%
- **Clear Cover:** 45% 20%
  - Designing: 27%
  - Machining: 9%
  - Fabrication: 9%
- **Assembly**: 10 % 5%
  - Fabrication: 10%

70% OF OVERALL ENCLOSURE GOAL COMPLETE

5.8 Structural Supports

Scintillator Support – 75% of Overall Task Goal

Subtasks:

• Scintillator Measurement – 10%	Complete	10/7/11
• Room Measurement– 10%	Complete	10/14/11
• Fastening Method Analysis – 50%	Complete	11/5/11
• Part Ordering-20%	TBD	
• Design Implementation – 10%	TBD	

70% OF OVERALL STRUCTURAL SUPPORT GOAL COMPLETE

6. Budget Estimate

D. Expense	Quantity	Unit Price $	Total $
Equipment			

Structural Support			
Beam Clamp 3/8”	4	2.39	9.56
Threaded Rod 3/8”	4	8.89	35.56
Hex Nut Full 3/8” 100PK	1	6.28	6.28
Flat Washer 3/8” 100 PK	1	5.09	5.09
Cooling System			
Peltier Cooler	2	7.50	13.00
Heat Pipe	1	41.00	41.00
Enclosure			
Acrylic Cover	1	68.57	68.57
Birch Plywood Baseplate	1	9.99	9.99
Total Equipment Cost			210.32
Total Project Cost			**210.32**

7. Overall Risk Assessment

7.1 Technical Risks:

7.1.1 Technical Risk 1: Structural system malfunction

If the system is installed incorrectly or there is an unforeseen force applied to the structural supports that exceed the safety factor added to each device then the system could fail i.e. break or collapse causing the devices to fall making falling object hazard to persons nearby possibly causing death or serious injury.
Probability : Moderate.
Solutions Add safety labeling

With routine structural inspection the strength and security of the supports can be ensured along with proper instruction and warning labeling.

7.1.2 Technical Risk 2: Datapath Malfunction

One technical risk associated with the datapath is a datapath malfunction. The data path may not function or fail to transmit and process data. Another malfunction could be parts of the old code are not integrated appropriately. <Probability: Low>
Inspect the code prior to saving a new top level design and testing it.

7.1.3 Technical Risk 3: Operational Frequency Issues

There is a chance that the chip will overheat faster than it can cool. This would result in the overheating of the board and possible failure of the program. <Probability: Likely>
The probability of this happening is likely because there has not been a lot of testing on the board when it is enclosed in the enclosure running at a fully operational frequency.
To prevent this there will be testing sessions and infrared thermometer readings to see what the heat produced is once the system is assembled.

7.2 Schedule Risks:

7.2.1 Schedule Risk 1: Datapath

One schedule risk associated with the datapath is the likelihood of untimely completion. If another datapath is not added in a timely manner, and new PMT/scintillator arrangement will not be able to be connected to the FEDM. The bit width of the datapaths have (to add room for another datapath) has already been shrunk ahead of schedule. Since this task has been completed early, the likelihood of the task being finished late is very low. <Probability: Very Low>

7.2.2 Schedule Risk 2: Structural Support Completion

The structural supports may not be completed in time due to the loss of a team member at a critical time. The needs of the customer have changed as well requireing a redesign to take place.The likelihood of this happening is moderate because the ordering of the parts will take some time and hasn't been ordered yet.
To solve this we will continue planning for the assembly of these parts so that when they arrive the fabrication of the structural design can be completed.

7.2.3 Schedule Risk3: Enclosure Completion

The enclosure may not be completed fast enough to get started on the actual mounting and thermal readings of the components. This will slow down the completion time of the other components that rely on the enclosure. <Probability: Moderate>
The likelihood of this happening is moderate because the ordering of the parts will take some time and hasn't been ordered yet.
To solve this we will continue planning for the assembly of these parts so that when they arrive the fabrication of the enclosure can be completed.

7.3 Budget Risks:

Not enough funding may be present which would prevent us from getting the parts for the enclosures, structural supports and cooling system in a timely manner. Not having these parts will prevent us from completing our project and halt our progress towards finishing the components.

8. Conclusion

The COSMICi system has been progressing at a timely rate. It should be completed on time according to the requirements of the Senior Design time requirements. Right now most components necessary to run the system have been designed and are now being fabricated. The design for physically installing the system set in its intended location has been determined. Once parts have been ordered, machined to specifications, and assembled, the system should run effectively acquiring data and display it on a readable display. This project will definitely meet its goal on time with a small possibility of continuing on to Phase 2.

9. References

http://cosmicinquirer.blogspot.com/
http://www-mariachi.physics.sunysb.edu/wiki/index.php/Main_Page

10. Appendices

POWER ANALYSIS

→Detector (2)
12V, 250mW
250mW/12V = 20.8mA, Measured current = 21mA

→FPGA Board
Voltage-5V
Current is 2A, allow for 3A
P=VI (5V)(3A)= 15W

→WIFI Board (2)
Voltage-5V, (USB)
Maximum measured current = .3A, allow for 50% of that .45A
P=VI (5V)(.45A) 2.25W

→DE3 Board
Voltage-3.3V
Max measured Current = .5A, Current drawn when program runs = .35A
P=VI (3.3V)(.5A)= 1.65W

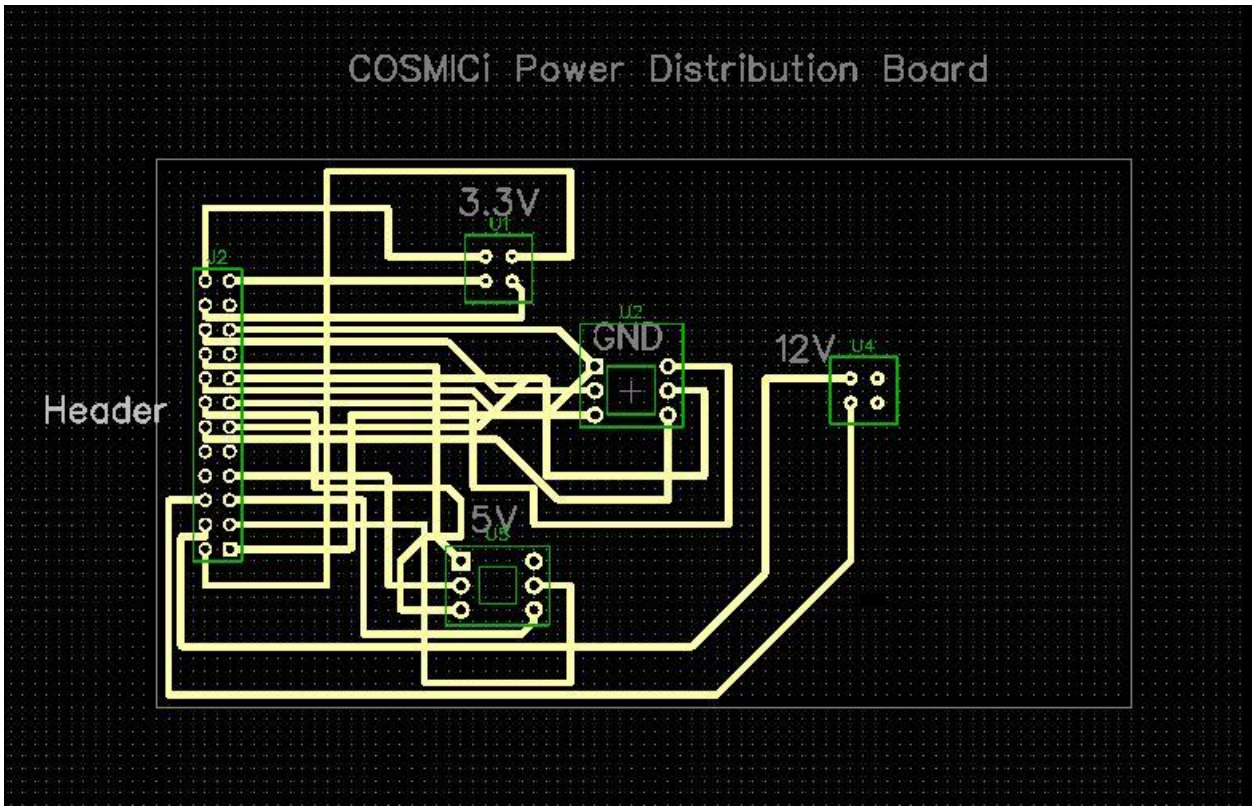
→Oscillator
Voltage-3.3V
Max measured current = .86A, Current drawn when program runs = .316A
P=VI (3.3V)(.86)= 2.83W

→GPS Kit
Voltage-5V (USB)
Max current for USB = 500mA
P= VI (5V)(.5A)= 2.5W

Total Power for all used components = **26.98W**

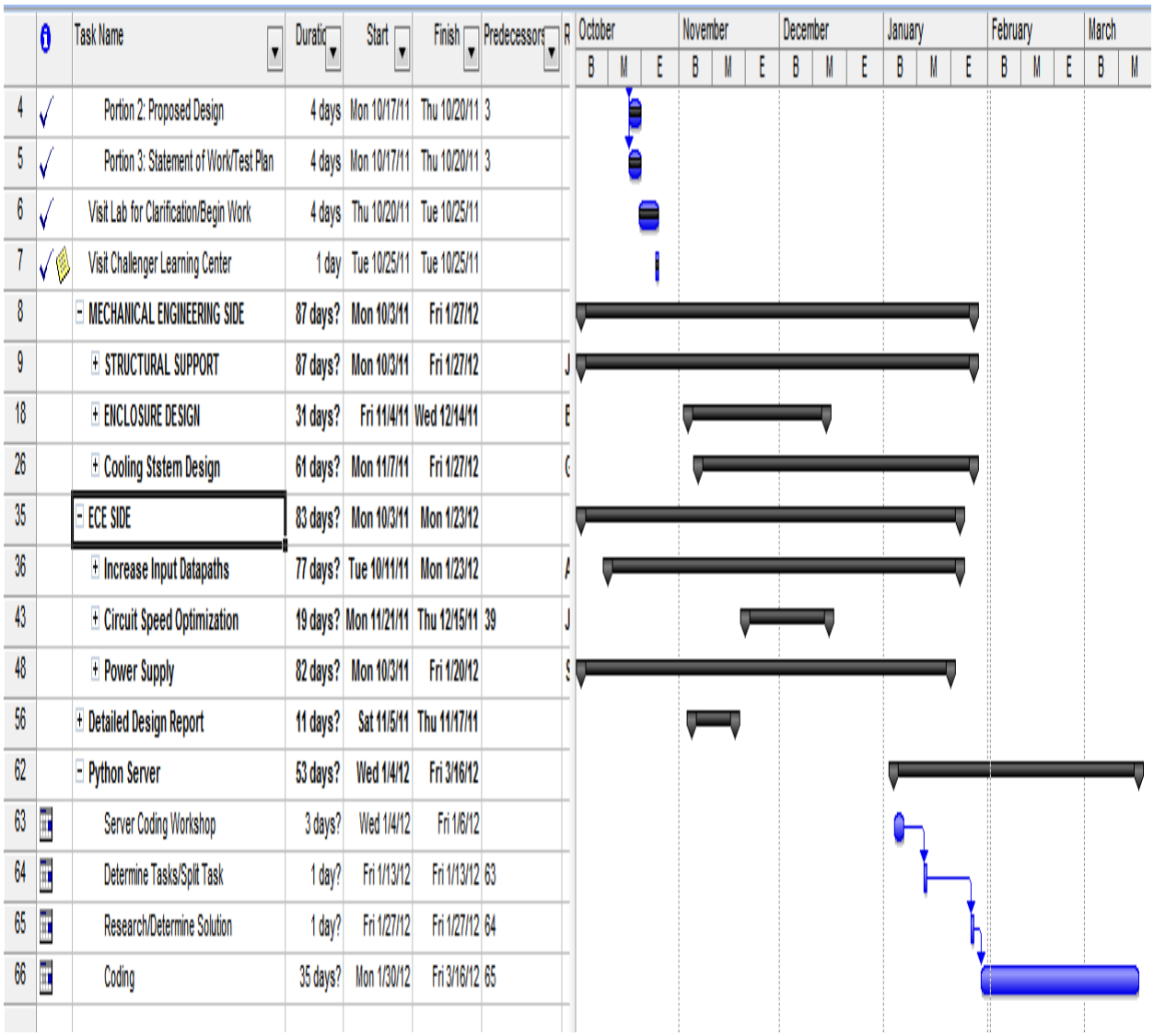
- This Lithium Ion Rechargeable Battery pack holds a voltage of 12V and has a recorded current of 4.5 Ahs. Our detector only requires a current of .021A.
  4.5Ah/.021A = 214.286 Hours.
  There are 168 hours in One week so… 214.286/168 = 1.27 weeks. Charging the battery every 1.27 weeks can become irritating. Using the same battery connected in parallel with a provided connector yields to the same output voltage. The battery's capacitance will change to 9Ah.
  9Ah/.021A = 428.57 Hours.
  428.57/168 = 2.55 Weeks. Charging the battery about every 2.5 weeks is more reasonable.

Schematic of PCB Board



Calculating the Internal Run time counter of the FEDM:
$2^{56} \times T \times 1min/60sec \times 1hour/60mins \times 1day/24hours$ = Number of Days before Timer Overflow
T = period of the FEDM code (Inverse of the operational frequency at 500MHz)

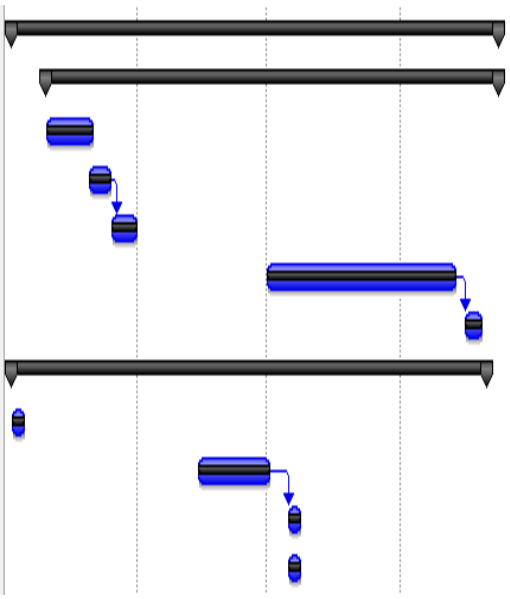
10.1 Schedule Update



	Task Name	Duration	Start	Finish	Predecessors
4	Portion 2: Proposed Design	4 days	Mon 10/17/11	Thu 10/20/11	3
5	Portion 3: Statement of Work/Test Plan	4 days	Mon 10/17/11	Thu 10/20/11	3
6	Visit Lab for Clarification/Begin Work	4 days	Thu 10/20/11	Tue 10/25/11	
7	Visit Challenger Learning Center	1 day	Tue 10/25/11	Tue 10/25/11	
8	MECHANICAL ENGINEERING SIDE	87 days?	Mon 10/3/11	Fri 1/27/12	
9	STRUCTURAL SUPPORT	87 days?	Mon 10/3/11	Fri 1/27/12	
18	ENCLOSURE DESIGN	31 days?	Fri 11/4/11	Wed 12/14/11	
26	Cooling Ststem Design	61 days?	Mon 11/7/11	Fri 1/27/12	
35	ECE SIDE	83 days?	Mon 10/3/11	Mon 1/23/12	
36	Increase Input Datapaths	77 days?	Tue 10/11/11	Mon 1/23/12	
43	Circuit Speed Optimization	19 days?	Mon 11/21/11	Thu 12/15/11	39
48	Power Supply	82 days?	Mon 10/3/11	Fri 1/20/12	
56	Detailed Design Report	11 days?	Sat 11/5/11	Thu 11/17/11	
62	Python Server	53 days?	Wed 1/4/12	Fri 3/16/12	
63	Server Coding Workshop	3 days?	Wed 1/4/12	Fri 1/6/12	
64	Determine Tasks/Split Task	1 day?	Fri 1/13/12	Fri 1/13/12	63
65	Research/Determine Solution	1 day?	Fri 1/27/12	Fri 1/27/12	64
66	Coding	35 days?	Mon 1/30/12	Fri 3/16/12	65

10.1.1 Completed Tasks – ECE Side

35		ECE SIDE	83 days?	Mon 10/3/11	Mon 1/23/12	
36		Increase Input Datapaths	77 days?	Tue 10/11/11	Mon 1/23/12	
37	✓	Review current code	9 days	Tue 10/11/11	Fri 10/21/11	
38	✓	Creat plan to decrease width	3 days	Fri 10/21/11	Tue 10/25/11	
39	✓	Decrease Width	4 days	Wed 10/26/11	Mon 10/31/11	38
40	✓	Add Input	32 days?	Thu 12/1/11	Fri 1/13/12	
41	✓	Check for errors	4 days?	Mon 1/16/12	Thu 1/19/12	40
48		Power Supply	82 days?	Mon 10/3/11	Fri 1/20/12	
49	✓	Provide Power for FEDM	3 days	Mon 10/3/11	Wed 10/5/11	
50	✓	Alternative Power Solutions	13 days	Tue 11/15/11	Thu 12/1/11	
51	✓	Research Solution	3 days	Tue 12/6/11	Thu 12/8/11	50
52	✓	Feasibility Study	3 days	Tue 12/6/11	Thu 12/8/11	



10.1.2 Completed Tasks – ME Side

8		MECHANICAL ENGINEERING SIDE	87 days?	Mon 10/3/11	Fri 1/27/12	
9		STRUCTURAL SUPPORT	87 days?	Mon 10/3/11	Fri 1/27/12	
10	✓	Idea Generation Phase	8 days	Mon 10/3/11	Wed 10/12/11	
11	✓	Idea Evaluation	1 day	Tue 10/18/11	Tue 10/18/11	10
12	✓	Feasible Approaches	1 day	Wed 11/9/11	Wed 11/9/11	11
18		ENCLOSURE DESIGN	31 days?	Fri 11/4/11	Wed 12/14/11	
19	✓	Get PCB sizes	1 day	Fri 11/4/11	Fri 11/4/11	
20	✓	Get approx cooling system size	1 day	Fri 11/11/11	Fri 11/11/11	19
21	✓	Design system	9 days	Sat 11/12/11	Wed 11/23/11	20
22	✓	Material Selection	7 days?	Sat 11/12/11	Mon 11/21/11	
26		Cooling Ststem Design	61 days?	Mon 11/7/11	Fri 1/27/12	
27	✓	Get board Measurments	1 day?	Mon 11/7/11	Mon 11/7/11	
28	✓	Get FPGA chip max running temp	1 day?	Mon 11/7/11	Mon 11/7/11	
29	✓	Design Sstem	2 days?	Mon 11/14/11	Tue 11/15/11	
30	✓	Find best metal for conduction/ material selection	1 day?	Mon 11/14/11	Mon 11/14/11	
31	✓	Design Calculations	5 days?	Mon 11/14/11	Fri 11/18/11	
32	✓	Order Materials	1 day?	Mon 12/5/11	Mon 12/5/11