EEL 4746: Microprocessor-based System Design

Chapter 11:
Analog Input and Output

Dr. Ming Yu
Dept. of ECE
FAMU-FSU College of Engineering
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11.1 Introduction

- To process continuous signals as functions of time
- Digital over Analog:
  - Advantages
    - Generally free of noise, not corrupted by dust and dirt
    - Can be manipulated by computers
  - Drawbacks
    - Analog signal can never be exactly represented or reconstructed by digital signal
    - Requires a greater bandwidth when transmitted over communication channel
    - The extra bandwidth is justified by being able to enhance the signal and to repeat it over long distances without degradation, and by opening the channel to other digital services such as data transfer between computers

11.2 Data Acquisition and Conversion

- A data acquisition system
  - Transducers:
    - convert the physical processes to electrical signals
  - Signal conditioning: functions are:
    - Isolation and buffering
    - Amplification
    - Bandwidth limiting
  - Analog multiplexer
    - Allow multiple analog inputs
    - Each with its own conditioning for different transducers
    - The multiplexer channel is selected by the CPU generating an address on the multiplexer select lines
  - Sample-and-hold
    - conversion time: the A/D converter requires a small but significant amount of time to convert.
    - If the analog signal changes during this time, errors may be introduced.
    - The sample-and-hold reduces these errors by quickly sampling the signal and holding it steady while the A/D converts it.

Figure 11-1 Data acquistion system.

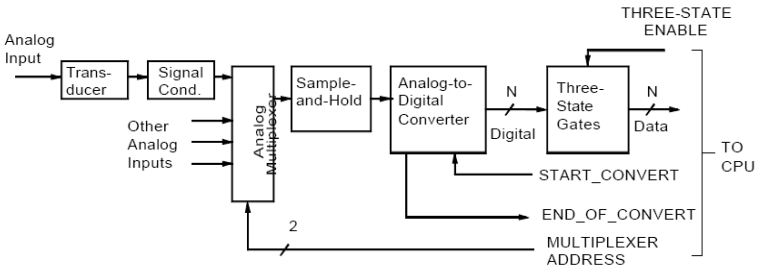
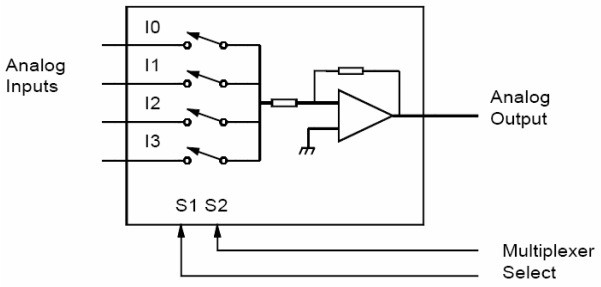


Figure 11-2 Analog signal multiplexer.



11.3 Shannon's Sampling Theorem and Aliasing

- The frequency at which signals are sampled must be at least two times the highest frequency in the signal

Sampling Frequency

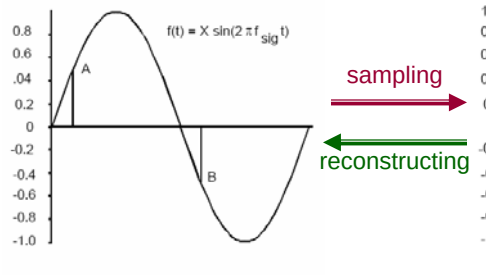


Figure 11-3 Sinusoidal waveform sampled at twice the signal frequency.

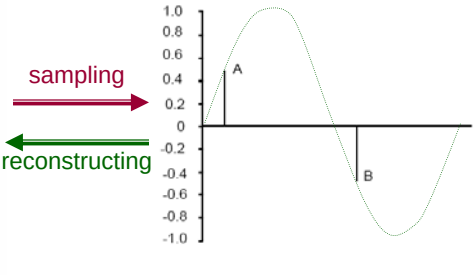


Figure 11-4 Sampled waveform.

f_sample >= 2 f_sig

Signals Undersampled Cause Aliasing

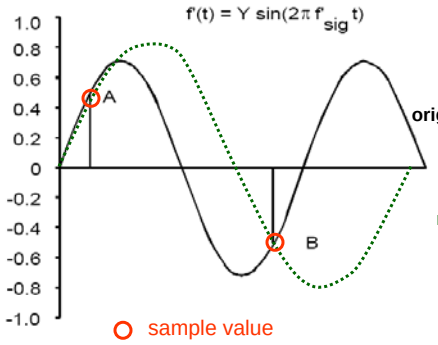


Figure 11-5 Undersampled waveform.

Antialiasing Filter: the signal conditioning stage must contain a filter to pass only low frequencies and attenuate frequencies above one-half the sampling frequency.

The one-half sampling frequency, $f_{sample}/2$, is called the **Nyquist freqency**, which must be greater than the maximum frequency component within the sginal to avoid aliasing.

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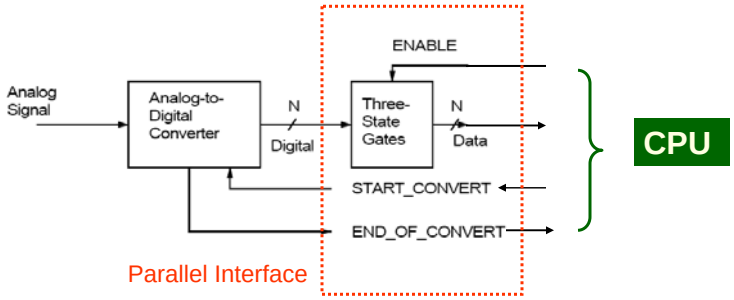
11.4 Analog-to-Digital Conversion

- A/D Converter Types
- A/D Converter Specifications
- A/D Errors
- Sample-and-Hold
- Choosing an A/D Converter

Figure 11-6 Analog-to-digital converter system.



The PI has a data bus and an address decoder to assert **THREE_STATE ENABLE** when the CPU is to read the converted data.

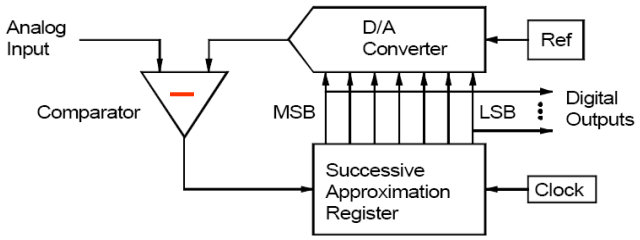
START_CONVERT: is asserted by the CPU to begin the conversion. This can be done with an output port bit or an address decoder.

END_OF_CONVERT: informs the CPU when the conversion is complete. This could be read as a status register bit in a polled I/O system or could generate an interrupt.

A/D Converter Types

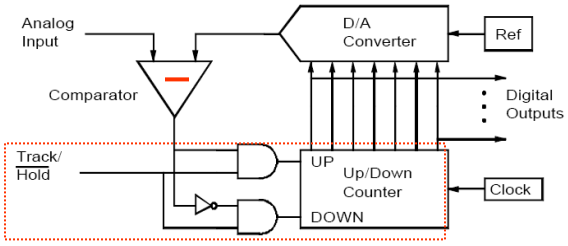
- Successive approximation A/D
- Tracking A/D Converter
  - or delta-encoded ADC
- Dual-slop A/D Converter
  - or multi-slope ADC, ramp-compare ADC, integrating ADC
- Parallel A/D Converter
  - or flash ADC
- Two-stage Parallel A/D Converter
  - or pipeline ADC, subranging quantizer
- Sigma-Delta ADC
  - or Delta-Sigma ADC
- Which one to choose?
  - Depends on the application and on the performance required

Figure 11-7 Successive approximation A/D.



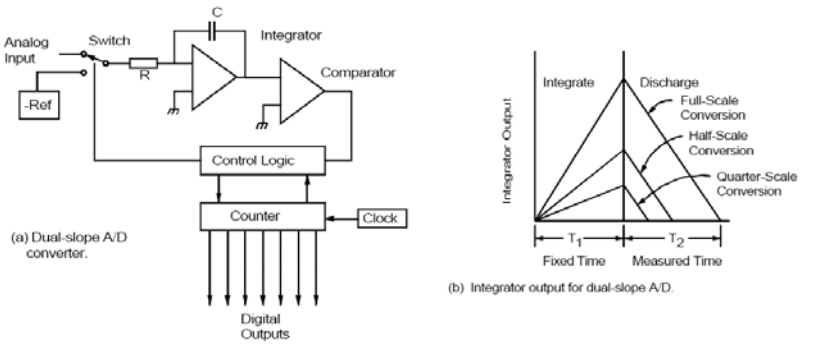
- Each bit in the SAR is tested, from the MSB to LSB.
- As each bit is set, the output of D/A is compared to the analog input.
  - If the D/A output is lower, then the bit remains set and try next bit.
  - If higher, the bit is reset.
- N bit-times are required.

Figure 11-8 Tracking A/D Converter.



- Compared to the successive approximation converter, it has an up/down counter controlled by the comparator.
  - If the input is higher or lower than the output of the D/A, the counter counts up or down.
  - This converter may quickly converges to the correct digital values if the signal is not changing rapidly.
    - If large, rapid, input changes are seen, the counter may have to count through its full range before reaching the final value

Figure 11-9 Dual-slope A/D converter.

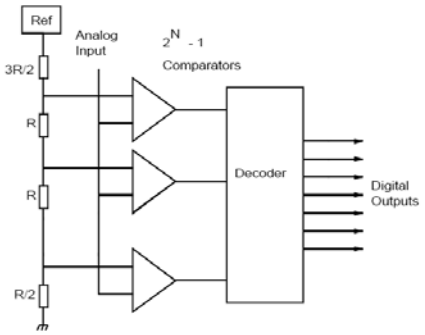


- The converter integrates the input signal for a fixed time, T1, with higher input signals integrating to higher values.
- During the second period, T2, the switch is changed to the minus reference voltage and integrator discharges to zero at constant rate.
- The time it takes to discharge, T2, gives the digital value.

How dual-slop ADC works?

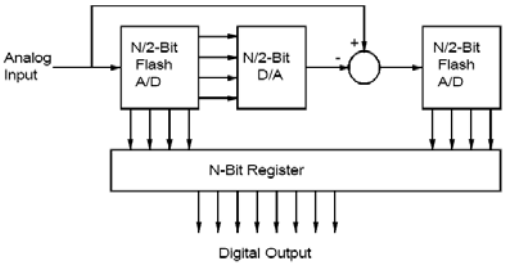
- Dual-slop ADC produces a saw-tooth signal that ramps up, then quickly falls to zero.
  - When the ramp starts, a timer starts counting.
  - When the ramp voltage matches the input, a comparator fires, and the timer's value is recorded, which is the digital value.
- Advantages:
  - Very efficient at recovering signals from periodic noise, such as the 60 Hz noise from power line.
    - By making T1 equal to the period of the interference (1/60 second), the positive half-cycle interference is canceled by the negative half-cycle.
  - Timed ramp converters require the least number of transistors
  - Comparing a second signal just requires another comparator, and another register to store the voltage value
- Disadvantages:
  - The ramp time is sensitive to temperature because the circuit generating the ramp is often just some simple oscillator
  - Two solutions:
    - use a clocked counter driving a DAC and then use the comparator to preserve the counter's value.
    - or calibrate the timed ramp

Figure 11-10 Parallel or flash A/D converter.



- It is an array of 2^N-1 comparators.
- Produces an output code in the propagation time of the comparators and the output decoder.
- Very fast but most costly.

Figure 11-11 Two-stage parallel A/D converter.



- Advantages:
  - Has nearly the performance of the parallel ADC but without the complexity of 2^N-1 comparators.
  - Offer high resolution and high-speed for application like video signal processing.

- The input signal is converted into two pieces:
  - First, a coarse estimate is found by the first parallel A/D.
  - This digital value is sent to the D/A and the summer, where it is subtracted from the original signal.
  - The difference is converted by the second parallel A/D
  - The result combined with first A/D is the digital value.

Delta-Sigma ADC

- Oversample the desired signal by a large factor and filters the desired signal band.
- Generally a smaller number of bits than required are converted using a Flash ADC after the Filter.
- The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter.
  - This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies.
- A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output.

A/D Converter Specifications

- Conversion Time
  - The time to complete the conversion
  - It establishes the upper signal frequency limit the can be sampled without aliasing.

$$f_{MAX} = 1/(2 \times \text{conversion\_time})$$

- Resolution
  - The number of bits in the converter
  - The smallest analog input signal for which the converter will produce a digital code

$$\text{Resolution} = \text{full-scale-signal} / 2^n$$

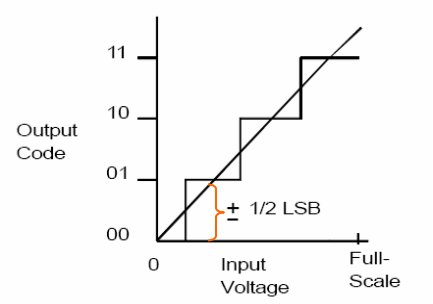
  - Often given as the number of bits, n, or stated as one part in 2^n. Sometimes given as a percent of maximum.
  - Resolution relates the smallest signal (or noise) to the full-scale signal
- Accuracy
  - Accuracy relates the smallest signal to the measured signal. The signal is accurate to within

$$V_{resolution} / V_{signal} \times 100\%$$

A/D Converter Specifications (2)

- Linearity
  - The deviation in output codes from a straight line draw through zero and full-scale.
  - The best that can be achieved is +-1/2 of the least significant bit
- Missing codes
  - Some output codes are missed
  - Caused by internal error, especially by the DAC in a successive approximation ADC
- Aperture time
  - The time that the ADC is “looking” at the input signal
  - Usually equal to the conversion time
  - Changes in the input signal during this time may cause an error in the output code

Linearity



Quantization levels

Figure 11-12 A/D linearity.

Missing Codes

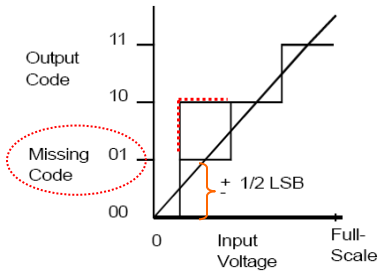
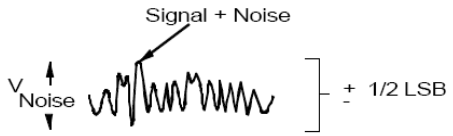


Figure 11-13 A/D missing codes.

A/D Errors

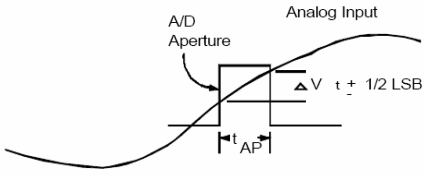
- The fundamental error in ADC is called the quantization error
  - due to the resolution of the ADC and
  - can be no less than +-1/2 LSB
- Sources of errors in ADC:
  - noise,
  - aliasing, and
  - aperture time

Figure 11-14 Analog signal plus noise.



- We would like the peak-to-peak noise to be less than + - 1/2 LSB
- Either choose the converter resolution appropriately or reduce the signal noise

Figure 11-15 Aperture time error.



- A significant error in digitizing is due to signal variation during the aperture time.
- The signal is changing when the aperture is open.
- A good design will attempt to have the uncertainty, ΔV, be less than one LSB.
- Design equation:

$$t_{AP} = \frac{1}{2\pi f_{MAX} 2^n}$$

Sample-and-Hold

- The sample-and-hold achieves the very short aperture time usually needed
- It's a high-quality capacitor and a high-speed semiconductor switch
  - The SAMPLE command closes the switch for a very short time
  - The capacitor charges or discharges to the input voltage
  - When the switch is open, the voltage is held fro the ADC during its conversion time

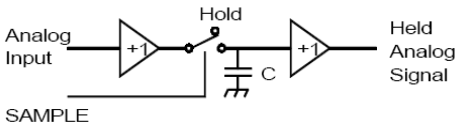


Figure 11-16 Sample-and-hold circuit.

Choosing an ADC

- Design issues
  - choose the number of bits, or resolution
  - the speed, or conversion time
  - the type of digital code output
  - the aperture time must be calculated and
  - a decision made to include a sample-and-held and an antialising filter in the system
- Choosing
  - A/D resolution
  - A/D conversion time
  - output code
  - sample-and-held

Choosing the ADC Resolution

- Method 1:
  - find the dynamic range of the input signal
  - choose the number of bits based on this
- Method 2:
  - based on the resolution required on the signal: V_{MIN}

Dynamic Range = $\frac{V_{MAX}}{V_{NOISE}}$

$$N \geq \log_2 \frac{V_{MAX}}{V_{NOISE}}$$

$$N \geq \log_2 \frac{V_{MAX}}{V_{MIN}}$$

Choosing an ADC (2)

- Choosing the A/D conversion time
  - By considering the potential signal aliasing
  - The highest frequency component in the signal must be sampled at least twice in a period
- Choosing the output code
  - depend on the input signal, different codes are available
- Choosing a sample-and-held
  - Almost any variable signal will require a sample-and-held, although there are sampling ADC that have the sample-and-held built in.

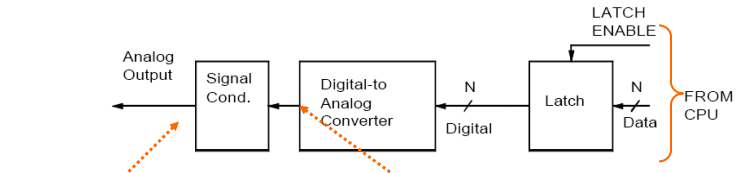
A/D conversion time $\leq \frac{1}{2 f_{MAX}}$

See Table 11-1 and 11-2

11.5 Digital-to-Analog Conversion

- DAC Types
  - The binary-weighted register DAC
  - R-2R Ladder DAC
  - Multiplying DAC
    - By using the reference voltage as an input
    - The reference voltage can vary over maximum voltage range of the amplifier and is multiplied by the digital code
- DAC Specifications
  - Resolution and linearity
  - Settling time
  - glitches

Figure 11-17 Digital-to-analog converter.



- Used as a filter to smooth the quantized nature of the output
- Also provide isolation, buffering, and voltage amplification if needed.

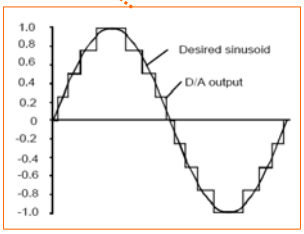
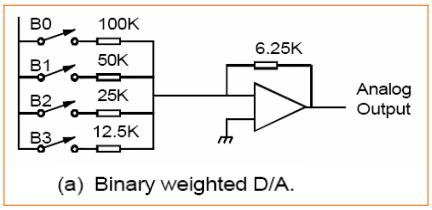


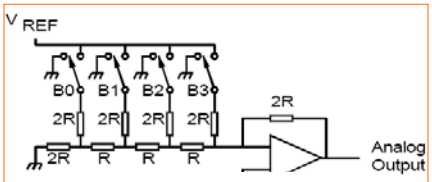
Figure 11-18 Quantized D/A output waveform.

Figure 11-19 D/A converters.



(a) Binary weighted D/A.

- The most basic circuit
- As the switches for the bits are closed, a weighted current is supplied to the summing junction of the amplifier
- For high-resolution DAC, the binary-weighted type must have a wide range of resistors. This can lead to the temperature stability and switching problem.



(b) R/2R ladder network D/A.

- Here, single-pole double-throw switches are required.
- As the switches are changed from the ground to the reference position, a binary-weighted current is supplied to the summing junction.

DAC Specifications: settling time

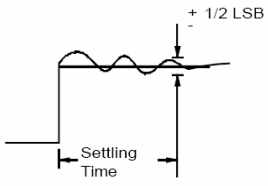


Figure 11-20 D/A settling time.

This is the time taken for the output to settle to within a specified error bound, usually + - ½ LSB.

DAC Specifications: glitches

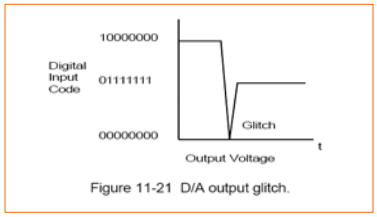


Figure 11-21 D/A output glitch.

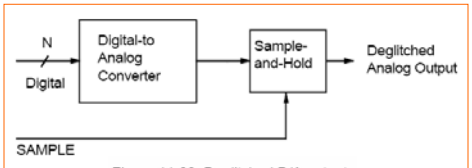


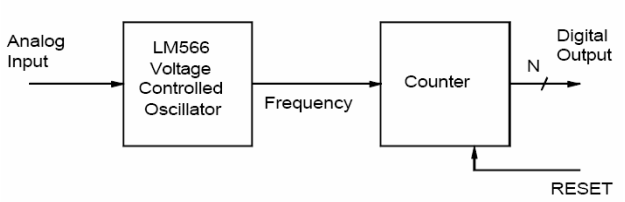
Figure 11-22 Deglitched D/A output.

- Caused by asymmetrical switching in the D/A switches
- Example:
  - if the switching from 1 to 0 is faster than 0 to 1, the state change from 10…0 to 01…1 will go to 00…0 first (transient) then goes to 01…1.
- Solution: glitches can be eliminated by following the D/A with a sample-and-held.
  - The S/H is strobed to sample the data after the glitch has occurred and after the D/A settling time.

11.6 Other Analog I/O Methods

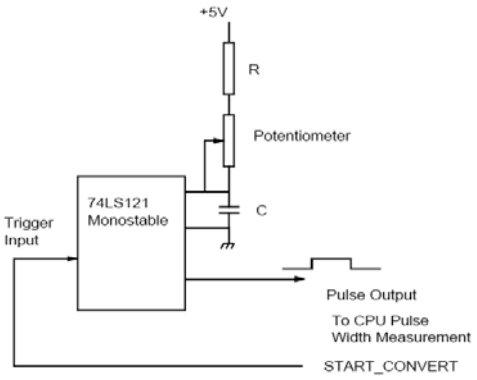
- Voltage-to-frequency converter (V-F)
  - Or voltage-controlled oscillator (VCO)
  - Produces an output frequency proportional to the input voltage
- Pulse-width-modulated analog input
- Pulse-width-modulate analog output

Figure 11-23 Voltage-to-frequency converter.



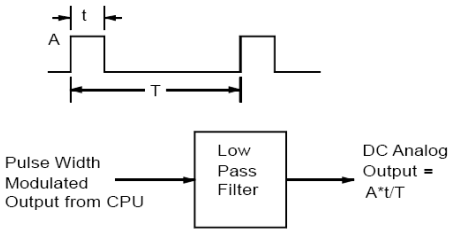
- The counter is set to zero at the start of the conversion cycle and read by the CPU a predetermined time later.
- The number in the counter gives the digital value, but the CPU must accurately wait for the prescribed amount of time.
- This technique is good for slowly varying signals or where an average value over a time is required.

Figure 11-24 Pulse-width modulation for analog input.



- In some cases, the position of a potentiometer may be the desired information. For example, a user may vary a control parameter by turning a knob on the front panel.
- if the potentiometer is not needed for another purpose, it can control the width of an output pulse of a monostable multivibrator.
- The width of the output pulse must be measured by the CPU.

Figure 11-25 Pulse-width modulation for analog output.



When the pulse train is low-pass filtered with a cutoff frequency of less than 1/T Hz, the output voltage is At/T.

11.7 Chapter Summary

- ADC Design Specifications
- DAC Design Specifications
- How to choose an ADC for an application?