- The branch instructions all use relative addressing.
- Always use the *JSR* instruction to jump to a subroutine.
- Condition code register bits may be used to transfer binary information between parts of a program.

4.18 Further Reading

There are two Motorola references that will help with your programming. The *M68HC11xxx Programming Reference Guide* is a pocket-size guide with all instructions and their symbolic operations, addressing modes, hexadecimal machine codes, the number of bytes, the number of clock cycles, and the effect on the condition code register. The *M68HC11 Reference Manual* contains details for programming all I/O in the M68HC11 and a complete listing of the instruction set.

4.19 Problems

4.1 For each of the following questions, assume the memory display of the M68HC11 shows:

C100 B0 53 05 2B 36 89 00 FF FE 80 91 3E 77 AB 8F 7F

Give the results after each of the following instructions is executed.

(a) LDAA $C100 A = ?, NZVC = ?

(b) Assume IX = $C100
LDAA 0,X A = ?, NZVC = ?

(c) Assume IX = $C100
LDAA 6,X A = ?, NZVC = ?

4.2 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

(a) LDX $C100 X = ?

(b) LDY $C102 Y = ?

(c) LDX $C103
PSHX
PULA
PULB X = ?, A = ?, B = ?

(d) LDD $C100
LDX $C102
XGDX D = ?, X = ?

(e) Assume IX = $C100
LDD $0A,X D = ?

4.3 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

(a) SP = $C105
PULA A = ?, SP = ?

(b) SP = $C105
PULA A = ?
PULB B = ?

(c) SP = $C105
PSHA
PSHB SP = ?

(d) SP = $C10A
PULA
PSHB A = ?, SP = ?

4.4 Why do store instructions not use the immediate addressing mode?

4.5 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

(a) Assume IX = $C100
BSET 0,X $0F ($C100) = ?

(b) Assume IX = $C100
BSET 6,X $AA EA = ?, (EA) = ?

(c) Assume IX = $C107
BCLR 0,X $AA ($C107) = ?

(d) Assume IY = $C100
BCLR 0,Y $FF ($C100) = ?

4.6 Assume A = $C9 and the NZVC bits are 0001. Give the result in A and the NZVC bits for each of the following instructions.

(a) LSLA; (b) LSRA; (c) ASLA; (d) ASRA; (e) ROLA; (f) RORA.

4.7 The ASLx instructions have the same operation codes as the LSLx instructions. Why?

4.8 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

(a) LDAA $C103
LDAB $C104
ABA A = ?, B = ?, NZVC = ?

(b) LDX $C100
LDAB $C107
ABX X = ?, NZVC = ?

(c) LDAB $C109
ADDB $C10A B = ?, NZVC = ?

(d) Assume IX = $C100
LDAA 9,X
ADDA $0A,X A = ?, NZVC = ?

(e) Assume IX = $C100
LDAA 9,X
SUBA $0A,X A = ?, NZVC = ?

(f) LDAA $C100
LDAB $C101
ABA
ADCA $C102 A = ?, NZVC = ?

4.9 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

```
(a) LDAA    $C106
    NEGA                A = ?, NZVC = ?
(b) LDAA    $C107
    NEGA                A = ?, NZVC = ?
(c) NEG     $C109       ($C109) = ?, NZVC = ?
(d) LDAA    $C106
    COMA                A = ?, NZVC = ?
(e) LDAA    $C107
    COMA                A = ?, NZVC = ?
(f) COM     $C109       ($C109) = ?, NZVC = ?
```

4.10 After an addition, the carry bit in a status register indicates that a 2's complement overflow has occurred—true or false?

4.11 The following straight binary addition was done in the M68HC11. What is the binary result and what are the N, Z, V, and C flags?

```
01010111
01100110
```

4.12 Assume the following M68HC11 code is executed in sequence. Give the hexadecimal result in each of the indicated registers after each instruction is executed.

	A	B	C	N	Z	V
ldaa #$4A	____	xxxx	—	—	—	—
ldab #$D3	xxxx	____	—	—	—	—
aba	____	____	—	—	—	—
adca #$70	____	____	—	—	—	—

4.13 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

```
LDAA    $C102
ADDA    $C104       A = ?
DAA                 A = ?
```

4.14 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

```
(a) LDAA    $C102
    ORAA    $C103   A = ?, NZVC = ?
(b) LDAA    $C102
    EORA    $C103   A = ?, NZVC = ?
(c) LDAA    $C10D
    ANDA    $C10E   A = ?, NZVC = ?
(d) LDAB    $C102
    COMB            A = ?, NZVC = ?
```

4.15 Use the contents of memory shown in Problem 4.1 and give the results of the following instructions.

```
(a) LDAA    $C100
    CMP     $C101   A = ?, NZVC = ?
(b) TST     $C106   NZVC = ?
(c) TST     $C107   NZVC = ?
```

4.16 Assume the ACCA = $00 and memory location DATA = $B0. A *CMPA DATA* in-

struction is executed followed by a conditional branch. For each of the conditional branch instructions in the table, indicate by yes or no if you expect the branch to be taken.

BGE	BLE	BGT	BLT	BEQ	BNE
BHS	BLS	BHI	BLO		

4.17 Assume the ACCA = $05 and memory location DATA = $22. A *CMPA DATA* instruction is executed followed by a conditional branch. For each of the conditional branch instructions in the table, indicate by yes or no if you expect the branch to be taken.

BGE	BLE	BGT	BLT	BEQ	BNE
BHS	BLS	BHI	BLO		

4.18 Assume the ACCA = $56 and memory location DATA = $22. A *CMPA DATA* instruction is executed followed by a conditional branch. For each of the conditional branch instructions in the table, indicate by yes or no if you expect the branch to be taken.

BGE	BLE	BGT	BLT	BEQ	BNE
BHS	BLS	BHI	BLO		

4.19 Assume the ACCA = $22 and memory location DATA = $22. A *CMPA DATA* instruction is executed followed by a conditional branch. For each of the conditional branch instructions in the table, indicate by yes or no if you expect the branch to be taken.

BGE	BLE	BGT	BLT	BEQ	BNE
BHS	BLS	BHI	BLO		

4.20 Briefly describe what each of the following instructions do. These are separate instructions, not a program.

COMA; CBA; CMPB 10,X; TSTB; BRN; SWI; BITA $80; BCC LOOP; XGDX; LSR $C100; NEGB

4.21 Example 4–25 shows how to use shift instructions to multiply by 10. Write an equivalent section of code using the MUL instruction and compare the time taken for the two.

4.22 Example 4–26 shows a comparison of the time it takes to do a multiply using the arithmetic shift versus using the MUL instruction. What advantage does using the MUL instruction give you?

4.23 Without using IDIV or FDIV, write a segment of M68HC11 code to divide the 16-bit, 2's complement integer number in the D accumulator by 10. Assume the quotient is to remain in D and the remainder is ignored.

4.24 Assume two 8-bit, two's-complement, integer numbers are in the A and B accumulators. Write a segment of M68HC11 code to multiply them.