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Scaling Trends in Adiabatic Logic

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Outline

- Adiabatic Logic Families:
  Fully or quasi-adiabatic?
- Choice of threshold voltage in multi-V_{th} technology
- Gate leakage
- Scaling of the supply voltage
- Conclusions

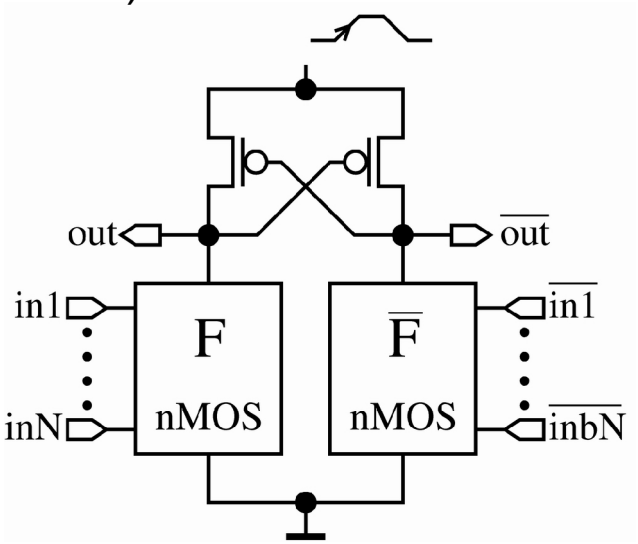
Quasi-Adiabatic Logic in Modern Technologies

- The prevailing opinion is, that only fully adiabatic families can save most energy.
- The dissipation of quasi-adiabatic families is limited by additional mechanisms,
  which mainly depend on the threshold voltage

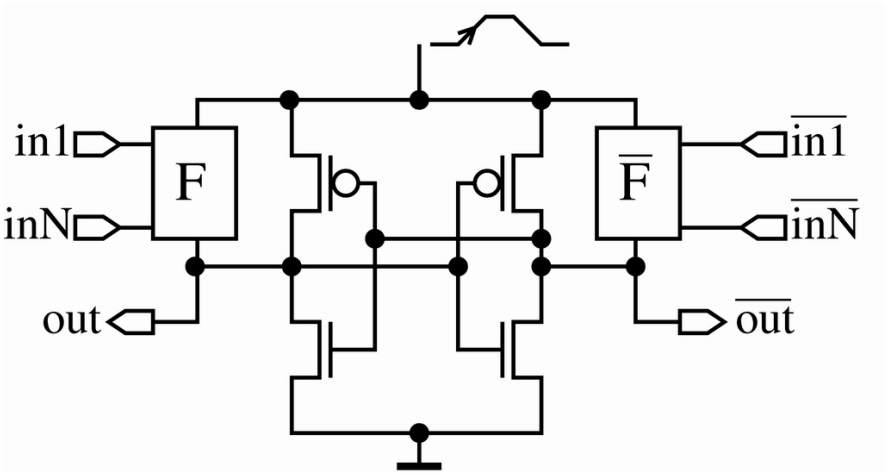
Do quasi-adiabatic logic families really dissipate more than fully adiabatic ones in modern technologies with reduced threshold voltages and increasing leakage currents?

Considered Adiabatic Logic Families

Efficient Charge Recovery Logic (ECRL)

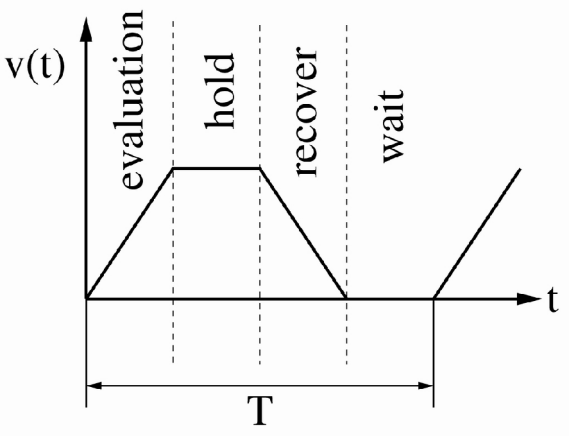


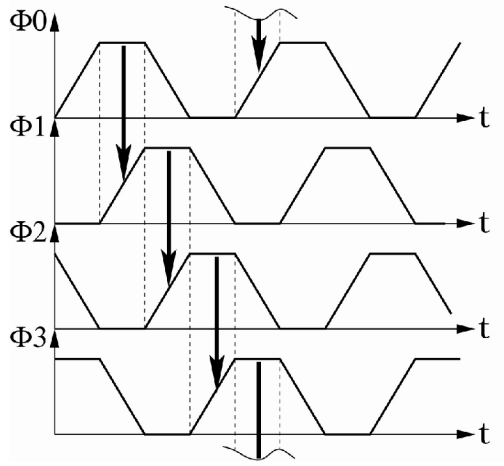
Positive Feedback Adiabatic Logic (PFAL)



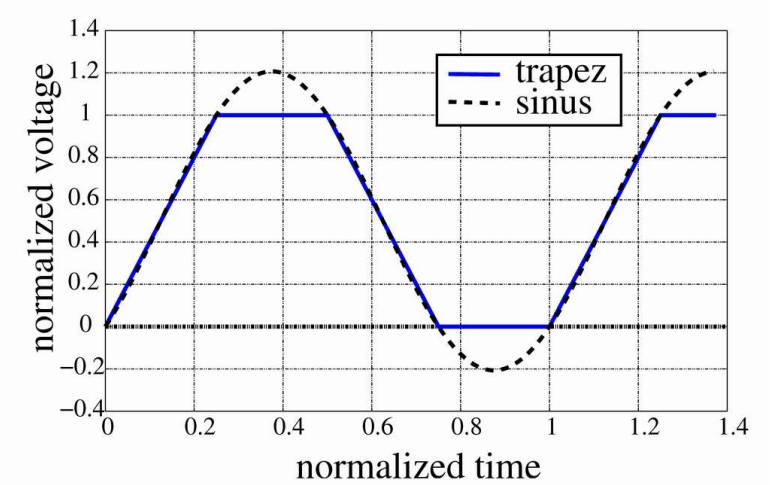
- Efficient Charge Recovery Logic:
  Lowest number of transistors
- Positive Feedback Adiabatic Logic:
  Function blocks assist adiabatic charging

Power Clock System



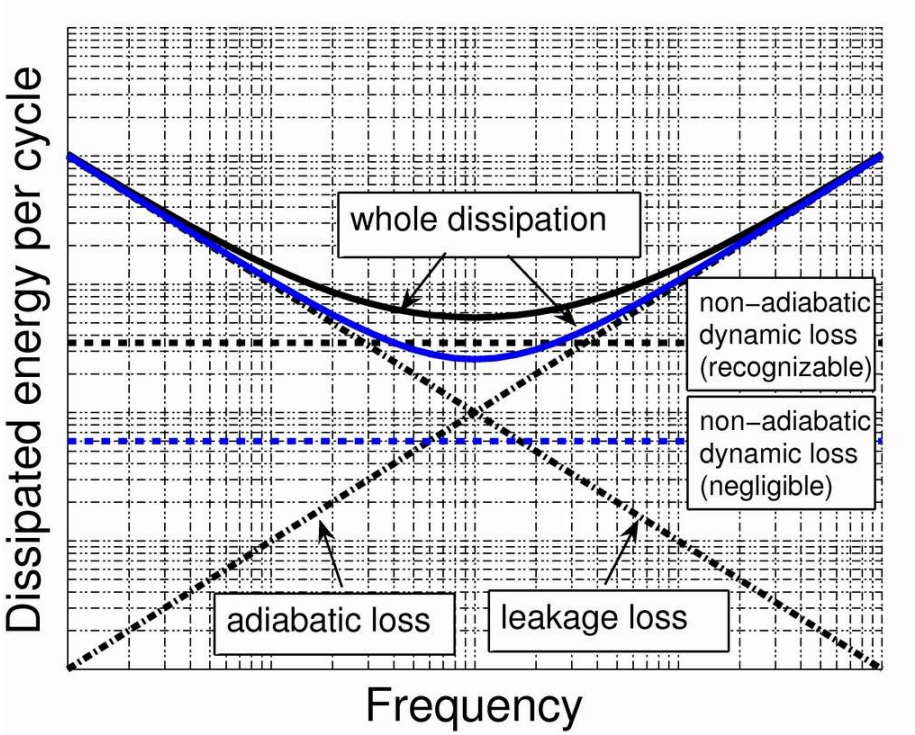


Ideal Power Clock signal has trapezoidal waveform.



Approximation of the trapezoidal waveform by a sinusoidal one

Sources of Energy Dissipation



- **Adiabatic loss**

$$E_{diss,adiab} = 4 \cdot f \cdot R \cdot C^2 \cdot V_{DD}^2$$

- **Leakage loss**

$$E_{diss,leakage} = V_{DD} \cdot \overline{I_{off}} \cdot f^{-1}$$

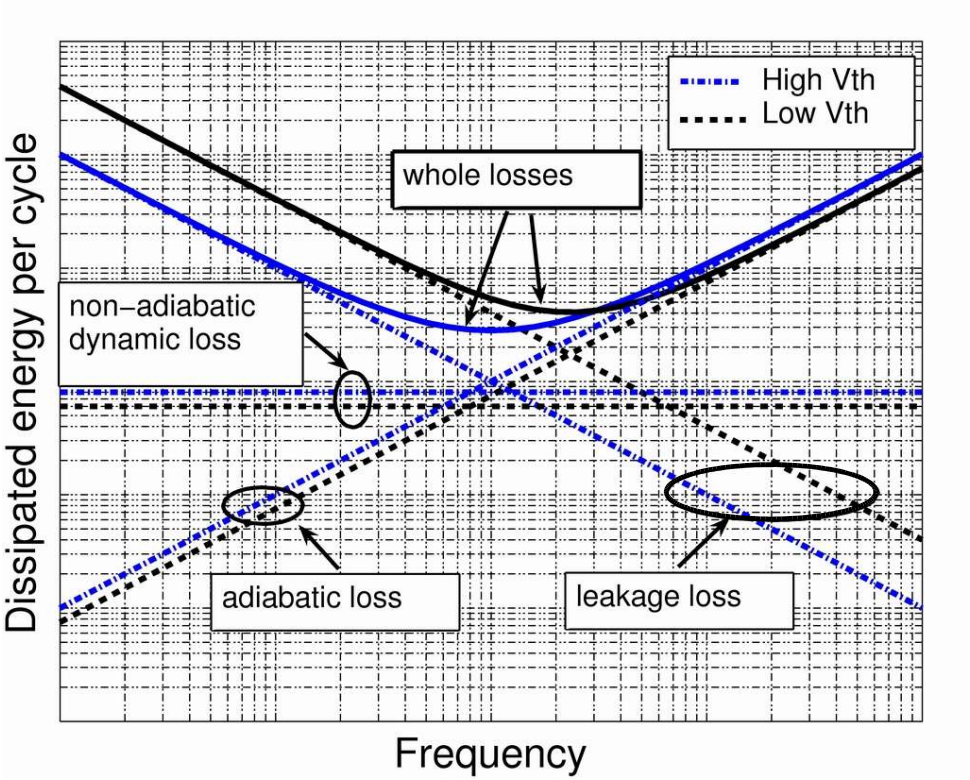
- **Non-adiabatic dynamic loss**
  - Voltage steps

$$E_{diss,Vth} = \frac{1}{2} \cdot C \cdot V_{th}^2$$

  - Coupling effects

Energy dissipation of static CMOS $E_{CMOS} = \frac{1}{2} \cdot C \cdot V_{DD}^2$

Scaling Threshold Voltage – Theory



High Frequencies:

Benefits from lower V_{th}, as

$$R_{on} \propto (V_{GS} - V_{th})^{-1}$$

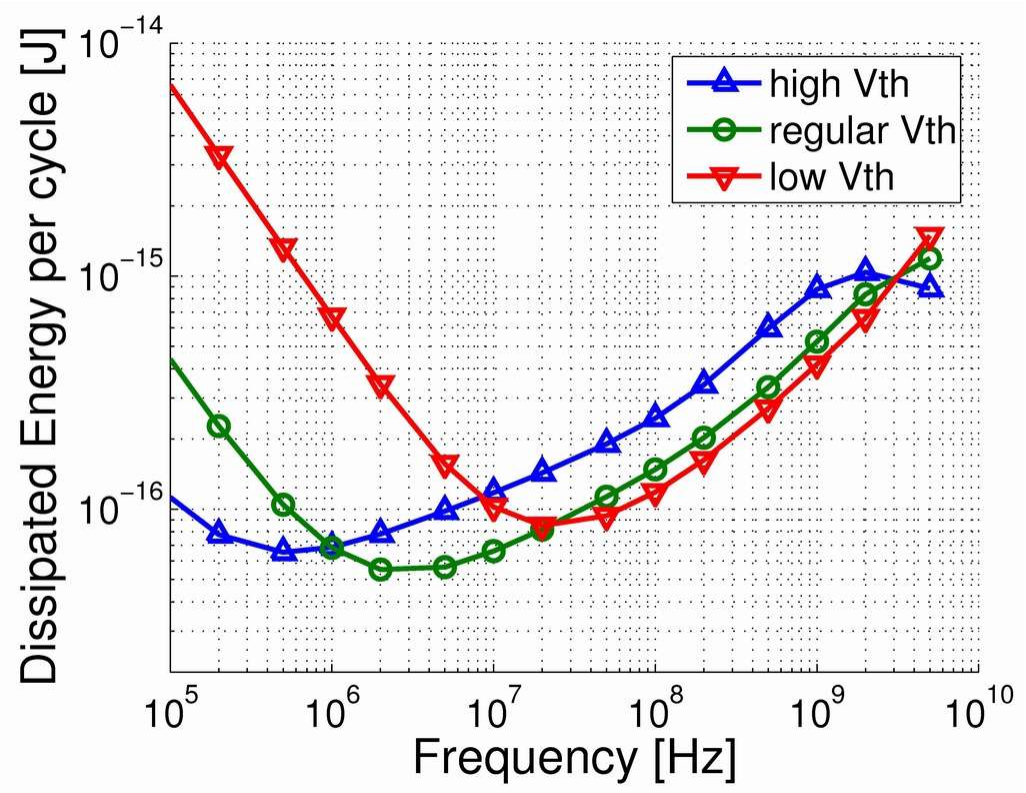
Low Frequencies:

Benefits from higher V_{th}, as

$$I_{sub} \propto \exp\left(-\frac{V_{th}}{nkT/q}\right)$$

If the non-adiabatic dynamic losses are negligible,
the overall minimum is found with higher threshold voltage.

Scaling Threshold Voltage – Simulation



Simulation of a PFAL inverter chain in a 130nm CMOS technology (V_{DD}=1.2V) with

high $V_{th} \approx 500mV$

regular $V_{th} \approx 400mV$

low $V_{th} \approx 300mV$

- At high frequencies low threshold voltage is preferable, at lower frequencies regular V_{th} and high V_{th}
- Overall minimum is found with regular V_{th}

$\Rightarrow$ For regular and low V_{th} non-adiabatic dynamic losses are negligible.

$\Rightarrow$ Quasi-adiabatic logic families show the same energy dissipation than full adiabatic ones.

Technology

- Main scaling parameters: $t_{OX}(\downarrow)$, W ($\downarrow$), L ($\downarrow$), V_{DD} ($\downarrow$), V_{th} ($\downarrow$)
- Impacts :

$$C = \frac{\epsilon_{OX} \cdot W \cdot L}{t_{OX}} \quad (\downarrow)$$

$$R \approx \left[\mu \cdot \frac{\epsilon_{OX}}{t_{OX}} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th}) \right]^{-1} \quad (\uparrow)$$

$\rightarrow$ altogether: RC (Transistor) ($\downarrow$)

- Energy dissipation of adiabatic logic:

$$E_{AL} \propto R \cdot C^2 \cdot V_{DD}^2$$

- Energy dissipation of static CMOS:

$$E_{CMOS} \propto C \cdot V_{DD}^2$$

- Break even frequency: $\frac{1}{16} \cdot \frac{1}{RC}$ ($\uparrow$)

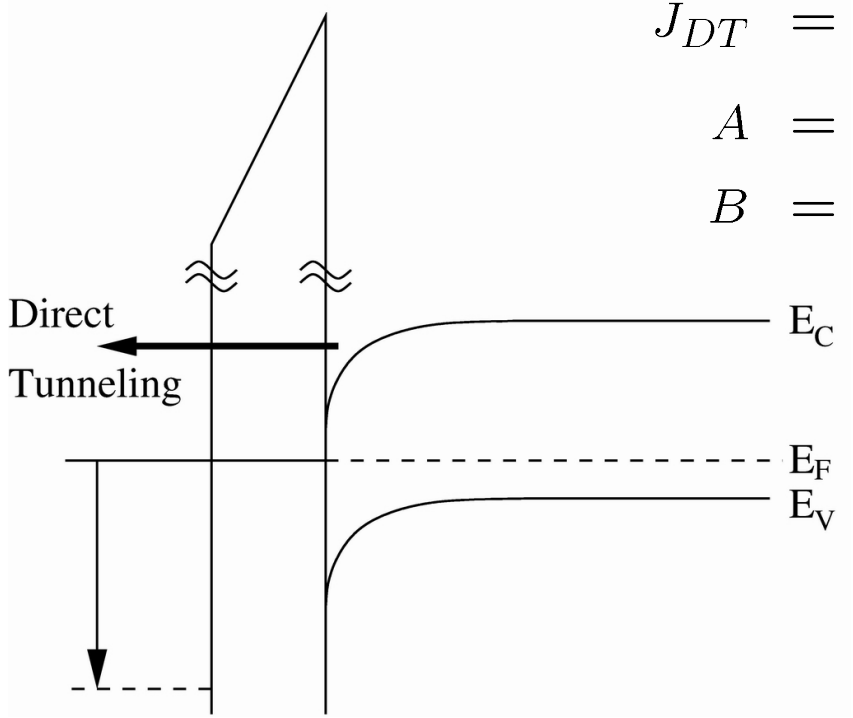
Gate Leakage

Direct Tunneling:

$$J_{DT} = AE_{ox}^2 exp\frac{-B\left[1-(1-\frac{V_{ox}}{\phi_{ox}})^{3/2}\right]}{E_{ox}}$$

$$A = q^3/16\pi^2\hbar\phi_{ox}$$

$$B = 4\sqrt{2m^*}\phi_{ox}^{3/2}/3\hbar q$$

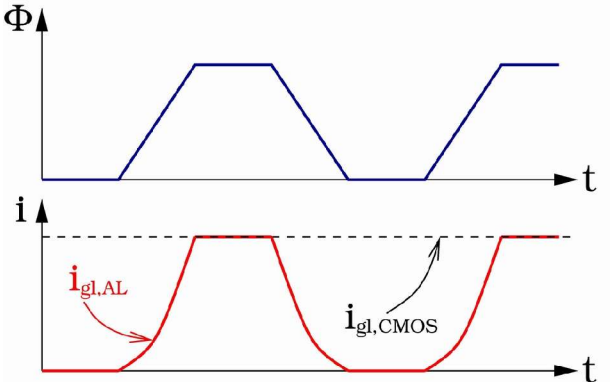


Gate leakage has become a recognizable effect with oxide thickness t_{OX} < 2nm,
i.e. for technology nodes of 90nm and beyond.

Energy Dissipation Factor

Figure of merit - Energy Dissipation Factor: $\eta = \frac{E_{gl,CMOS}}{E_{gl,AL}}$

Comparison of a single transistor



$$\eta = \frac{V_{DD} J_{DT}(V_{DD}) T}{\frac{8V_{DD}}{T} \int_0^{T/4} t J_{DT}(v(t)) dt + \frac{T}{4} V_{DD} J_{DT}(V_{DD})}$$

$$\eta^{-1} = \frac{\frac{8V_{DD}}{T} \int_0^{T/4} t J_{DT}(v(t)) dt}{V_{DD} J_{DT}(V_{DD}) T} + \frac{1}{4}$$

- Maximum supply voltage only one quarter of the period
- During rise and fall time also gate leakage currents are flowing.

$\Rightarrow \quad 2 < \eta < 4$

- Matlab simulation for a 90nm CMOS technology (V_{DD}=0.8V):

$\eta = 2.86$

Effective Energy Dissipation Factor

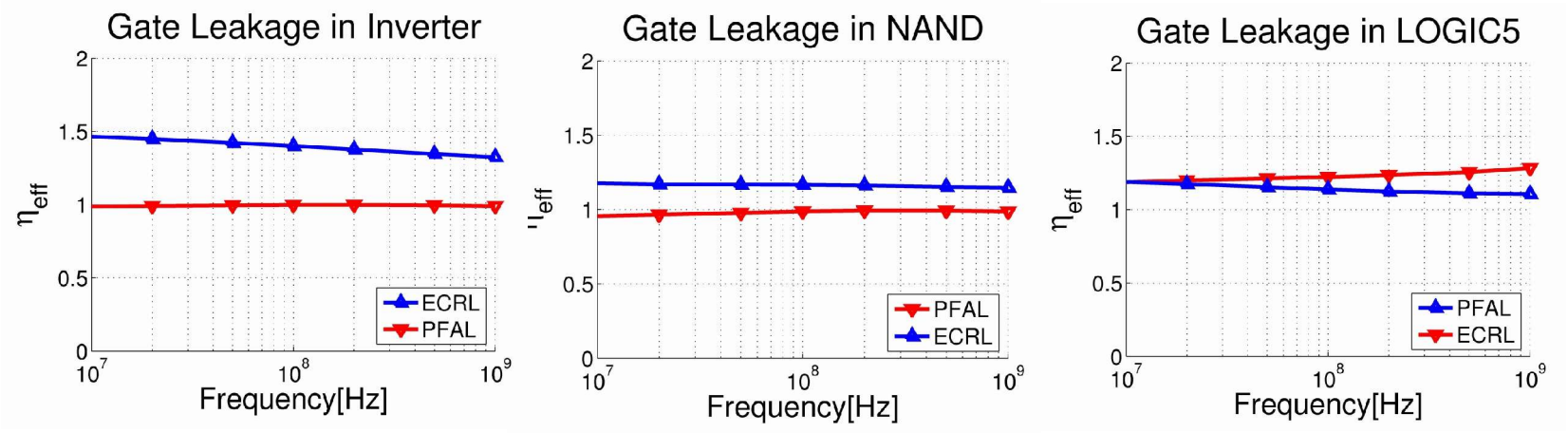
Effective Energy Dissipation Factor: $\eta_{eff} = \frac{\eta}{fn}$

	n_{CMOS}	n_{ECRL}	fn_{ECRL}	η_{eff} ECRL
INV	1	2	2	1.43
NAND	2	4	2	1.43
LOGIC5	5	10	2	1.43
	n_{CMOS}	n_{PFAL}	fn_{PFAL}	η_{eff} PFAL
INV	1	4	4	0.715
NAND	2	6	3	0.95
LOGIC5	5	12	2.4	1.19

$$fn = \frac{n_{AL}}{n_{CMOS}} = \frac{transistorcount_{n,AL}}{transistorcount_{n,CMOS}}$$

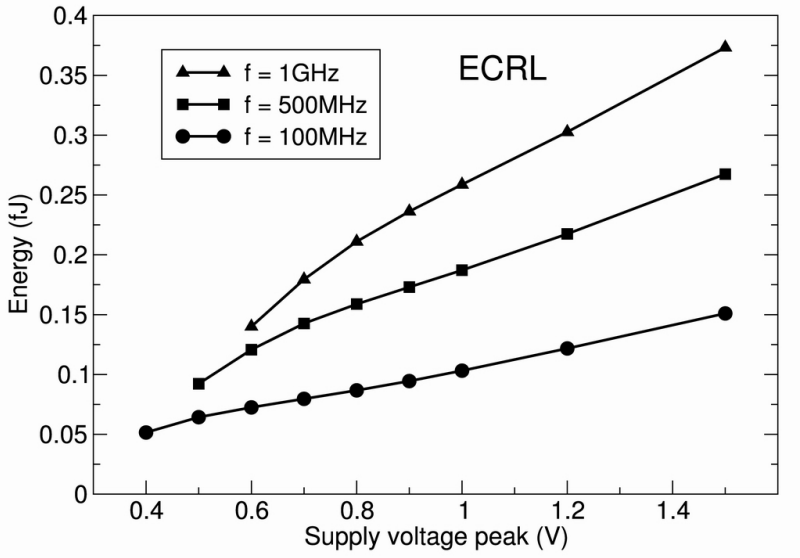
- Adiabatic logic gates contain more transistors than static CMOS
  → Effective Energy Dissipation Factor
- Gate leakage of n-channel MOSFET >> p-channel MOSFET
  → Only the n-channel transistor count is considered
- ECRL has twice n-channel transistors than static CMOS
- PFAL has two additional n-channel MOSFET than ECRL.
  The contribution of these transistors become less important for complex gates.

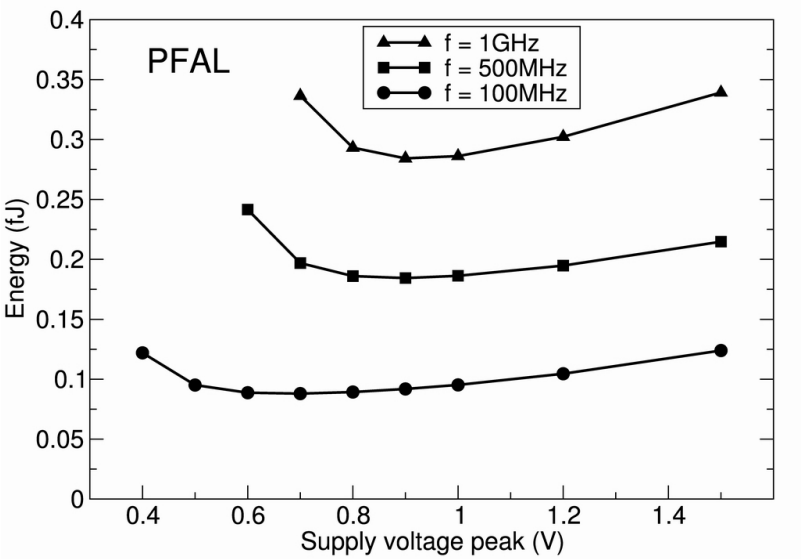
Gate Leakage – Simulations



- ECRL
  - Inverter: as estimated about 1.43
  - NAND/LOGIC5: about 1.25 because of additional effects, like stacking effects, position of logic blocks etc.
- PFAL
  - Inverter: better than estimated
  - NAND/LOGIC5: values as estimated

Scaling Supply Voltage





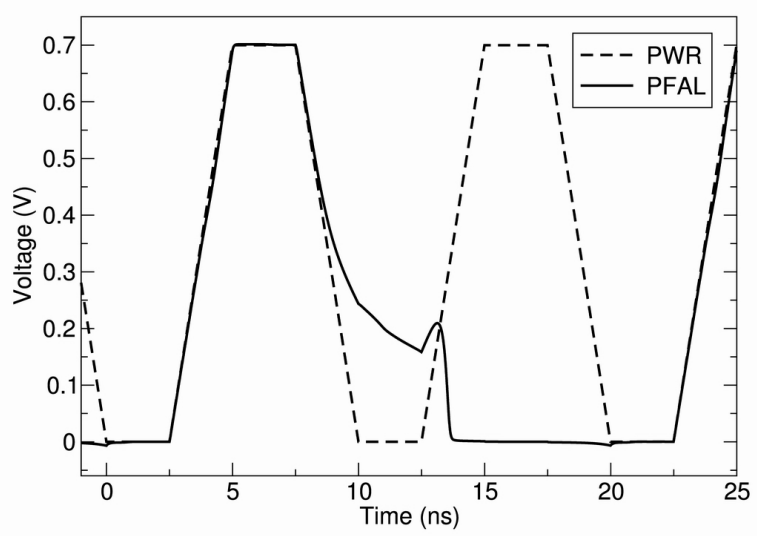
$$E_{adiab} = 4f \cdot R \cdot C^2 \cdot V_{DD}^2$$

$$\hookrightarrow R_{on} \propto (V_{GS} - V_{th})^{-1}$$

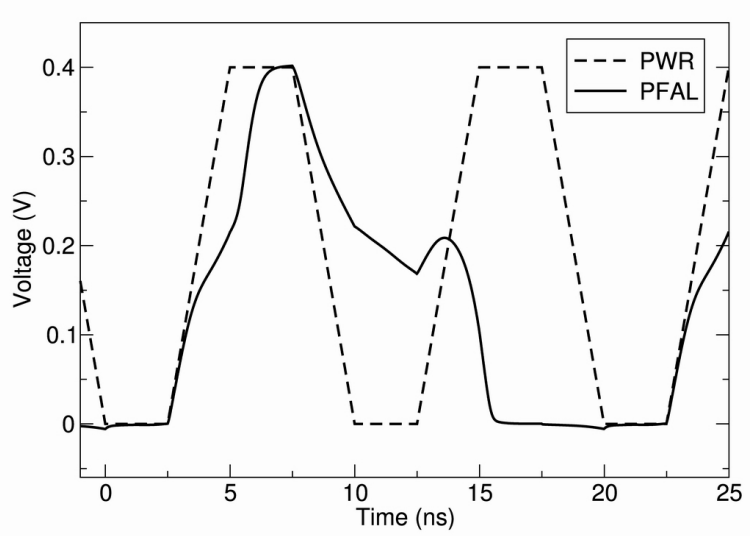
- ECRL scales linearly down to approx. V_{th}
- PFAL scales linearly down to approx. $2V_{th}$

Scaling of the Supply Voltage in PFAL

$V_{DD} = 0.7V \approx 2V_{th}$



$V_{DD} = 0.4V < 2V_{th}$

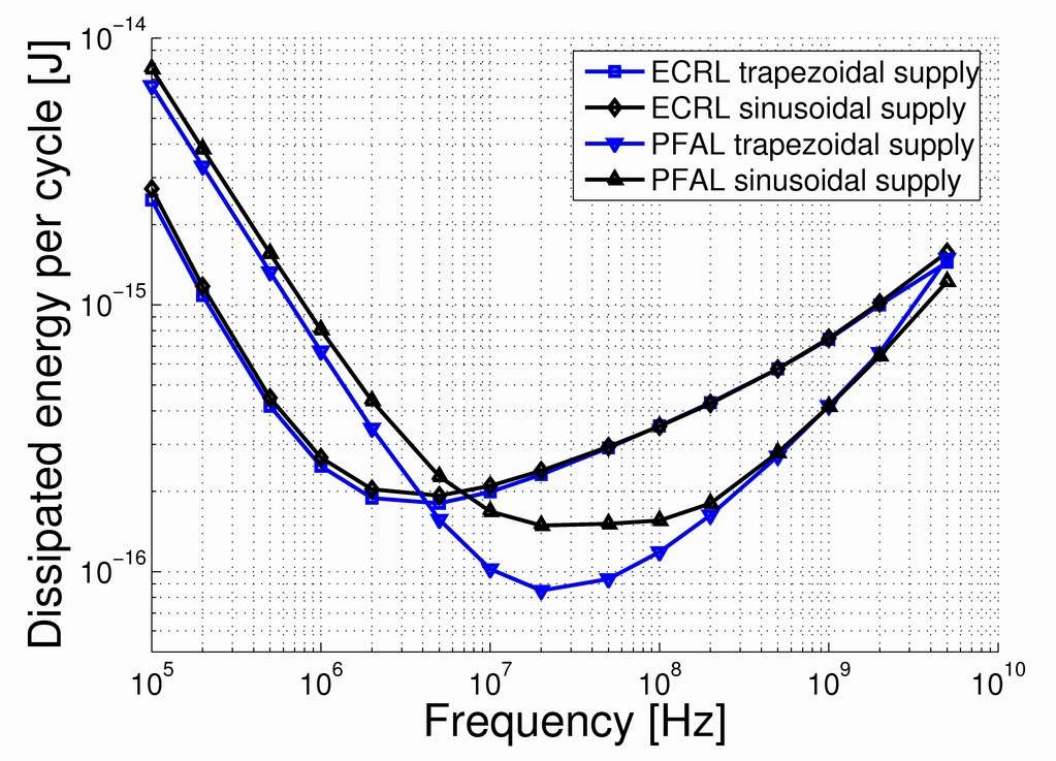


- Function blocks need a voltage drop of approx. V_{th}
- Latch needs a voltage drop of approx. V_{th}

$\rightarrow$ For supply voltages $V_{DD} < 2V_{th}$ the function blocks switch off before the latch begins to work

$\Rightarrow$ Increased energy dissipation

Trapezoidal vs. Sinusoidal Supply Voltage



- In real circuits the adiabatic logic is supplied with a sinusoidal voltage.
- No effect on the adiabatic energy dissipation (high frequencies)

Conclusions

- Non-adiabatic dynamic losses are negligible in modern technology
  ⇒ Quasi-adiabatic logic families behave like full-adiabatic ones
- Adiabatic logic gates benefit from technology scaling as well as static CMOS.
- Energy dissipation due to gate leakage comparable to static CMOS
- The supply voltage of ECRL can be scaled down to the threshold voltage.
- The adiabatic losses are not affected by a sinusoidal power supply.

ECRL shows the best properties for ultra-low voltage applications.
PFAL offers large energy savings at frequencies about 100MHz.