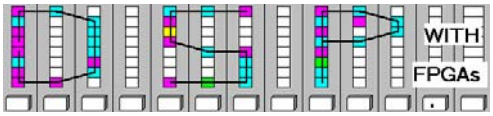
Lastname: _____

5Digit SS:_____

LABORATORY
Number Systems and Quantization



LAB : NUMBER SYSTEMS AND QUANTIZATION
(10 points)

In this lab you will be introduced to fractional number systems.
In the **pre-lab** you will compute via "pencil-and-paper" the results you later expect in your design implementation. In the **design part** you will design and simulate a 5-bit bus implementation of a fractional number system.

Lab Objectives

After completing this lab you should be able to

- understand the difference of signed and unsigned numbers systems
- determine minimum and maximum values in integer and factional number systems
- compute quantization error
- design and simulate a circuit using Simulink

Pre-lab (3 points)

1. The A/D converter used in our board uses a 12 bit integer **signed** data format.

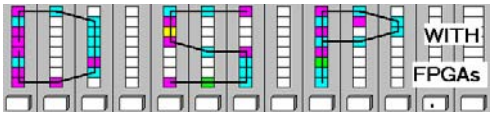
   a. Determine the maximum number that can represented: X_{max} =_____

   b. Determine the minimum number that can represented: X_{min} =_____

2. The D/A converter used in our board uses a 14 bit integer **unsigned** data format.

   c. Determine the maximum number that can represented: Y_{max} =_____

   d. Determine the minimum number that can represented: Y_{min} = _____



3. For the following signed fractional numbers with 3 integer and 2 fractional bits determine:

   a. the decimal weight (+/-2^k) for each digit in the signed 3.2 format:

   ___ ___ ___ . ___ ___

   b. the largest positive number in binary format B_{max} =_____

   c. the equivalent of B_{max} as decimal number D_{max} =_____

   d. the smallest positive number in binary format: $B_{smallest}$ = _____

   e. the equivalent of $B_{smallest}$ as decimal number $D_{smallest}$ = _____

   f. the minimum negative number in binary format: B_{min} =_____

   g. the equivalent of B_{min} as decimal number D_{min} =_____

4. the table values below for the 3.2 format (rounding: truncation)

Decimal Value	Binary 3.2 format	Decimal 3.2 equivalent	Quantization error (Dec. equivalent-Dec. Value)
2.5	__ __ __ . __ __		
-1.75	__ __ __ . __ __		
1/8	__ __ __ . __ __		
7/3	__ __ __ . __ __		
D_{max}=	__ __ __ . __ __		
D_{max}+ $D_{smallest}$ =	__ __ __ . __ __		

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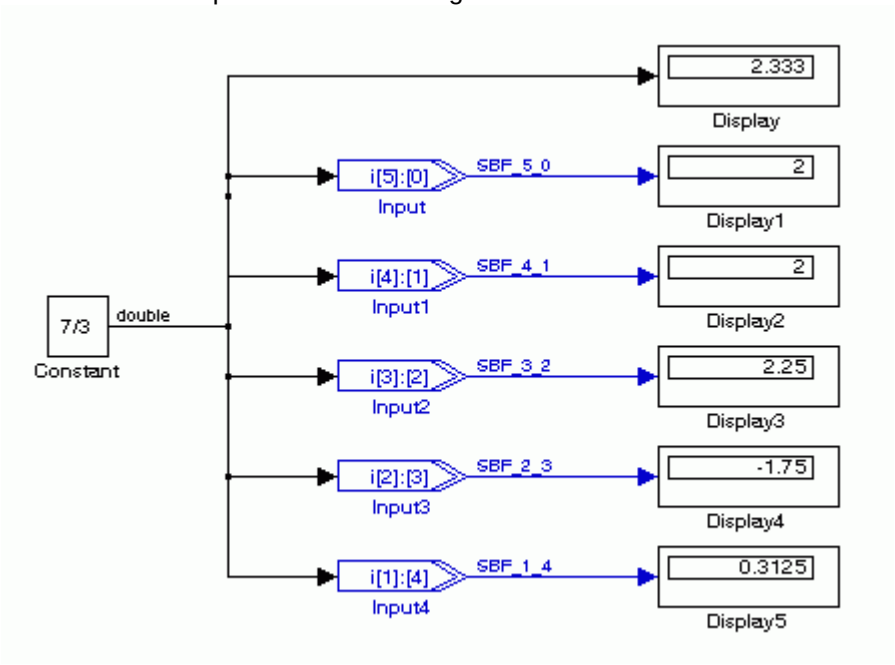
Simulink Design-lab

Follow the directions below to implement the following circuit:



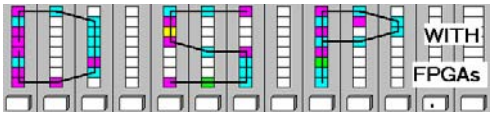
A. Getting Started

If you are in B114 or the digital logic lab:

1. On the desktop double click on **Engineering folder**.
2. Double click on **MatLab** icon  to start **MatLab**.
3. From the to top icon list in the **MatLab** window click on the **Simulink** icon  to start **Simulink.**
4. You should not save anything on the local hard disk. You will have to use an USB drive, a floppy disc, or your "mapped" home directory to save the files. Create or use the folder named **DSPwFPGAs** on your mapped network drive.

B. Creating Your Simulink Design

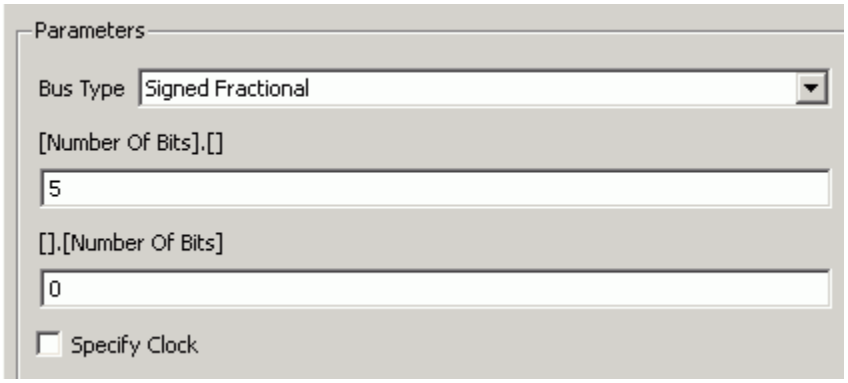
1. Select **New Model** from the **File** menu or click on the **New Model** button in the **Simulink Library Browser**.
2. From the **Simulink Library Browser** choose the **Simulink** library and click on **Sources**. Choose the **Constant** source and drag it into your worksheet or click on the source and use **CTRL+I** to add it to the worksheet automatically.



3. To add the inputs, go to the **Altera DSP Builder** library, then **IO & Bus**. Choose the **Input** block and place 5 of them in your worksheet, or add one Input block and use **Copy & Paste** to add the remaining 4 inputs.

4. Wire the **Constant** source to each of the inputs by connecting wires from the output of the source to the inputs. This can also be done by clicking on the source, pressing **CTRL**, then using the left mouse key to click on the inputs to generate multiple wires from the same source.

5. To change input type and number of bits in each input, double click on one of the **Input** blocks. Change **Bus Type** to Signed Fractional and click on the Apply button. Then change the **[Number Of Bits].[]** value to 5 and the **[].[Number Of Bits]** value to 0 as shown below:



6. Repeat above step for the remaining inputs and change the bits to [4].[1], [3].[2], [2].[3], and [1].[4].

7. Go to **Sinks** in the **Simulink** library and choose the **Display**. Use the default Format: short. Place 6 of them in your worksheet, or add one block and use **Copy & Paste** to add the remaining.

8. Wire the **Display** blocks to the output of the **Input** blocks and the **Constant** block.

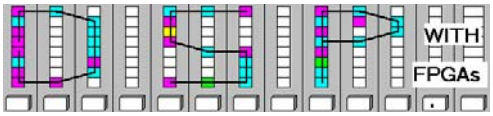
9. Save your design using **Save as** from the **File** menu.

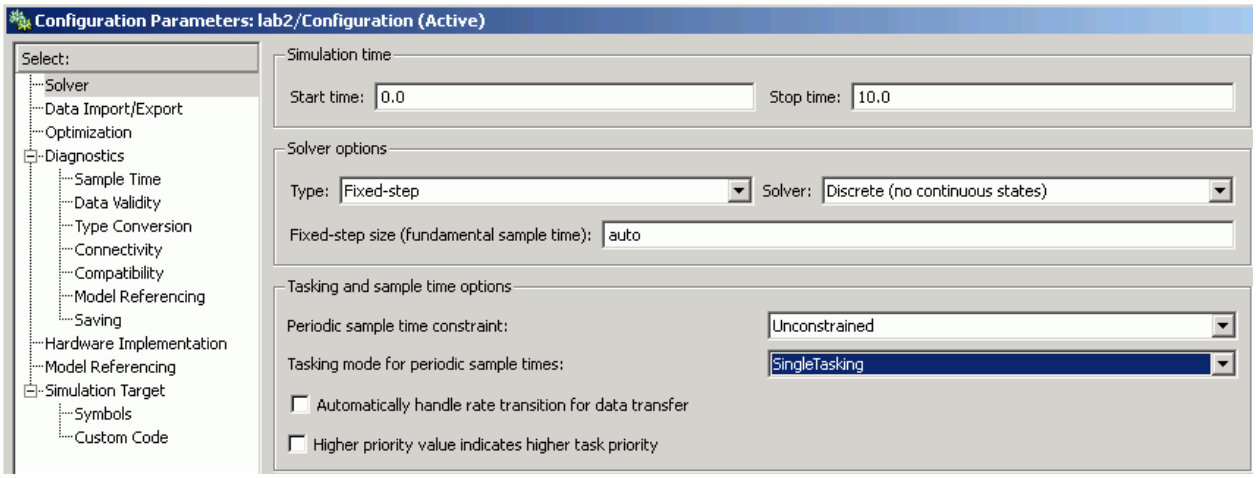
C. Simulating your Design

1. Double-click on the **Constant** source and change the **Constant Value** to 7/3.

2. On the menu bar go to **Simulation** and choose **Configuration Parameters** or use **CTRL+E** to change the parameters. Choose the following parameters as shown below:

   Type: Fixed-step
   Solver: Discrete (no continuous states)
   Tasking mode for periodic sample times: SingleTasking



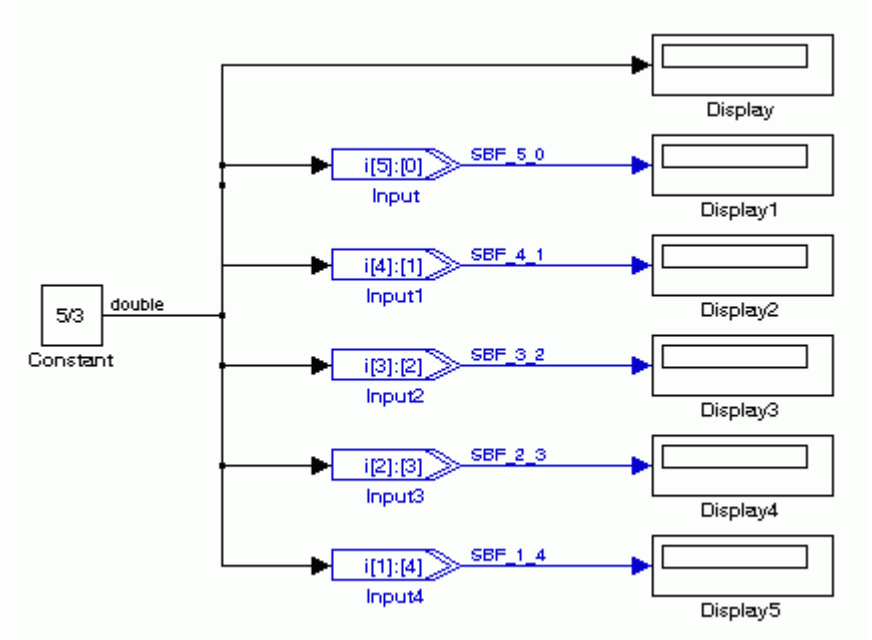


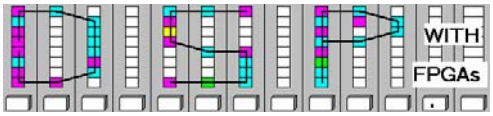
3. To simulate click on the **Start Simulation** button, choose **Start** under the **Simulation** menu, or use **CTRL+T**.

4. Complete the following table for values close to the boundary conditions for the 3.2 format with **Quantization: Truncate.** Compare your results with the pre-lab data.

Constant Value	Display	Error (Display-Value)	Overflow (yes/no)
3.75			
4.0			
-4			
-4.25			

5. Repeat steps 1 and 2 for a **Constant Value** of 5/3, and fill out the empty Displays below with the results:





D. Deliverables:

1. Solve the problems from the pre-lab. (3 points).
2. Print the MDF file (after simulation). (7 points)

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