LAB 5: Introduction to Finite Impulse Response Filters
(10 points)
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In this lab, you will be introduced to finite impulse response (FIR) filter design. Filters are one of the most important elements in DSP and are typically used to isolate a specific frequency band of a signal. FIR filters have low quantization sensitivity, simple structures, and can easily be made to have a linear phase response.

In the **pre-lab,** you will use "pencil-and-paper" to compute the results you expect later in your design implementation. In the **design part,** you will design a halfband filter using direct coefficient coding and reduced adder graph design. Please bring your own pair of headphones to the lab so you can hear the effects of noise and filtration.
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Lab Objectives

After completing this lab you should be able to

- Design and simulate an moving average filter (MAF)
- Understand the difference between the direct-form and transposed-form of an FIR filter
- Design and simulate a reduced adder graph FIR filter using Simulink
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Pre-lab (3 points)

For a moving average filter with K-taps, what should the output scaling be so that the overall gain of the filter is 1?

$\qquad$**Gain for K-tap MAF   =   _____**

What output scaling factor is required for a 4-tap MAF?

$\qquad$**Gain for 4-tap MAF   =   _____**

1. For a 3-tap MAF, determine the output values $y[n] = (x[n] + x[n-1] + x[n-2])/3$ for the input values given below. Assume zero values ($x[n],y[n]=0$) for $n<0$ and $8<n$.

N	0	1	2	3	4	5	6	7	8
x[n]	0	4	4	2	-1	-5	-3	-4	1
y[n]									

Do you think the original signal ($x[n]$ without noise) was a sine, cosine, triangle, or square wave?

2. Draw the impulse response using "stair functions" for the following halfband filter.
   (Coefficient values: $f[0] = f[10] = 9, f[2] = f[8] = -44, f[4] = f[6] = 208, f[5] = 348$)
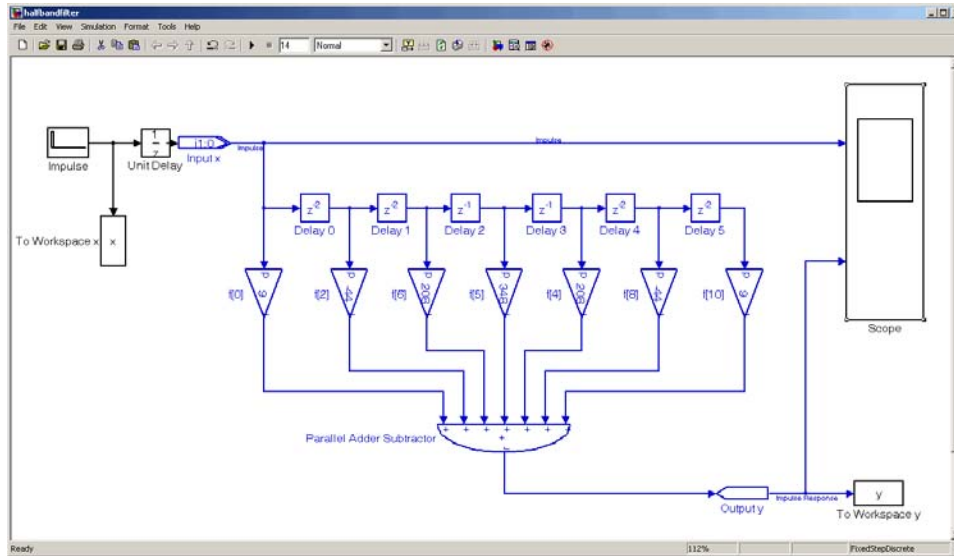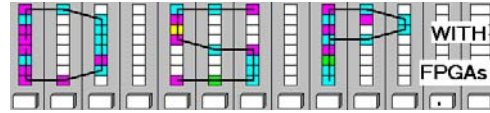
LABORATORY
FIR Filters

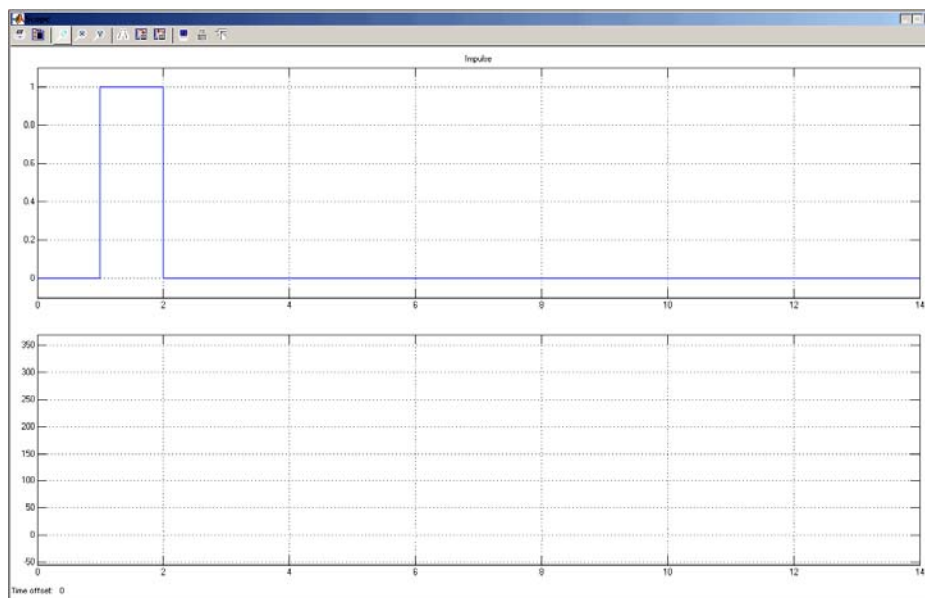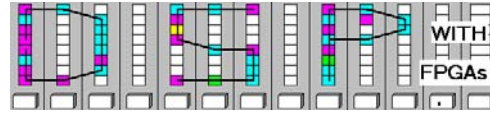
Figure 1: Halfband Filter

Figure 2: Scope plot for impulse response

3. Determine the reduced adder graph (RAG) for the F5 length-11 halfband filter with the following coefficients: $f[0] = f[10] = 3$, $f[2] = f[8] = -25 = -(3*8+1)$, $f[4] = f[6] = 150 = 25*3*2$, and $f[5] = 256$)

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Simulink Design-lab (7 points)

Follow the directions below to implement a moving average filter and a halfband filter.

A. Getting Started

If you are in B114 or the digital logic lab:

1. On the desktop double click on **Engineering folder**.

2. Double click on **MatLab** icon to start **MatLab**.

3. From the top toolbar in the **MatLab** window, click on the **Simulink** icon to start **Simulink.**

4. You should not save anything on the local hard disk. You will have to use a USB flash drive, or your "mapped" home directory to save the files. Create (if not done in a previous lab) a new folder named **DSPwFPGAs** on your mapped network drive.

B. Compiling an Existing Moving Average Filter Design

1. Download the file "**maf.mdl**" from the class webpage and put the file in your **DSPwFPGAs** folder.

2. On the **MatLab** toolbar, click on the "browse for folder" icon and select your **DSPwFPGAs** folder as the new directory.

3. The files in the **DSPwFPGAs** can now be easily accessed with the "open file" button on the **MatLab** toolbar. Double click on the "**maf.mdl**" file and after a moment you should see the design:
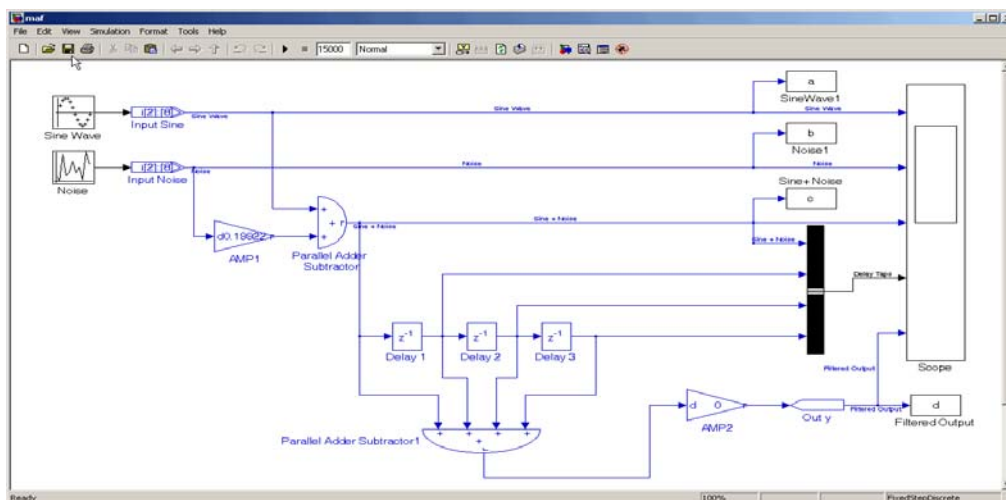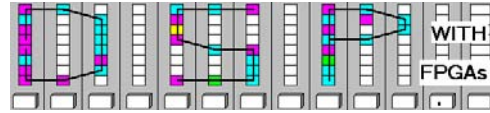

Figure 4: 4-tap moving average filter

4. Modify the gain of "AMP2" so that the overall gain of the system is 1 using the data from the pre-lab. Carefully choose the number of bits in the gain block by double-clicking on the gain block, selecting "Signed Fractional" as "Map Gain Value to Bus Type," and entering your value in "[].[Gain Value Number of Bits]." Verify the correct function by simulating your design and viewing the scope output.

5. The amplitude of the random noise generator amplitude is initially set to 0.2 (by "AMP1"). Press the "start simulation" button ▶ and look at the scope output. To hear the effects of noise and filtration, plug headphones into the headphone jack (at the back of the computer) and compare the noise signal with the filtered signal by typing the following 2 lines at the **MatLab** prompt:

> wavplay(c)
> wavplay(d)

Now, set "AMP1" to 0.9 and repeat. Can you hear the difference in the noise level?
(Note: At the **MatLab** prompt, simply press the "up" button to retype the last command.)

6. What is the maximum noise amplitude this MAF can tolerate such that the output is clearly a sine function? Use the scope to verify your guess. (**Print** and turn in the scope output for both an acceptable noise level and an unacceptable noise level.)
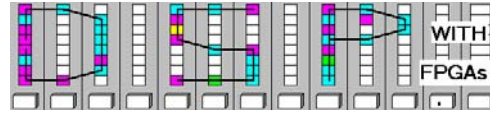
Maximum Noise Amplitude = _____

C. Simulating the F5 Direct-Form Filter

1. Download "**F5direct.mdl**" and "**showfft.m**" from the class webpage and put these files in your **DSPwFPGAs** folder. Open the "**F5direct.mdl**," and you should see the following design:
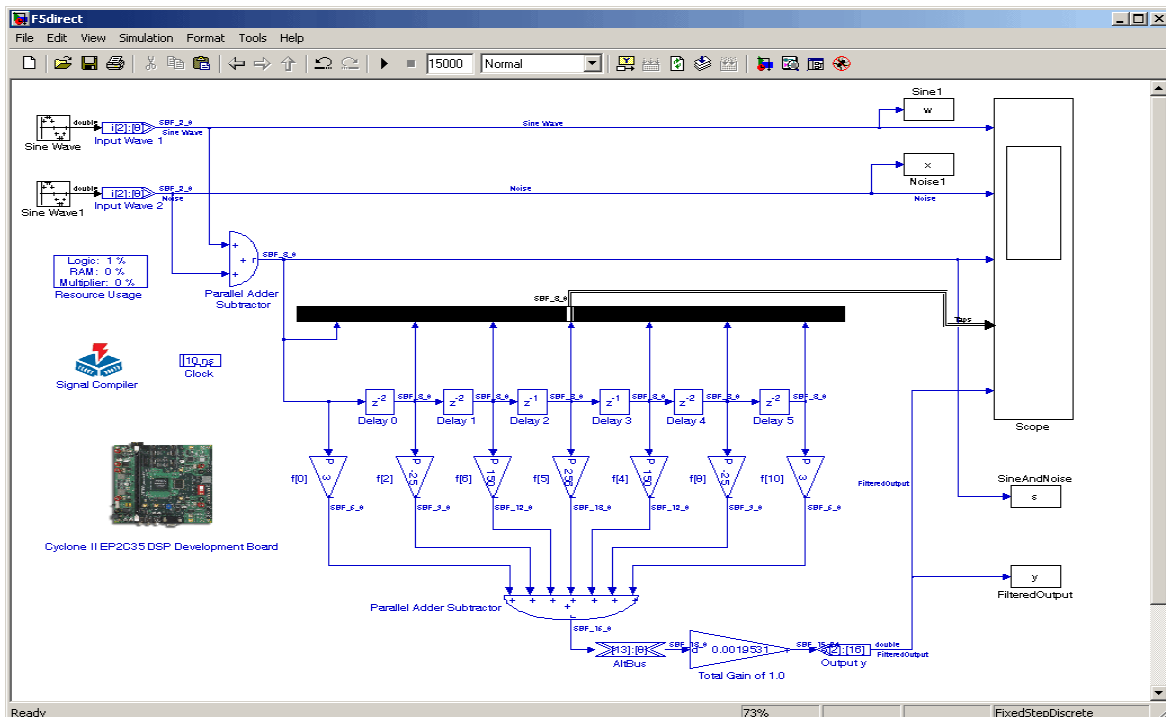
Figure 5: F5 Direct Filter

2. Simulate "**F5direct.mdl**." (**Print** and turn in scope output.)

3. At the **MatLab** prompt, use the `showfft(s)` and `showfft(y)` function provided to "measure" the amplitude of the "noise" sine component before and after filtering.

Noise Magnitude Before Filtration = _____

Noise Magnitude After Filtration = _____

4. For an acoustic comparison of the noise signal with the filtered signal type the following 2 lines at the **MatLab** prompt:
> wavplay(s)
> wavplay(y)

5. Determine the number of logic elements, DSP 9x9, and the minimum slack of the device:

Logic Cells = _____

DSP 9x9   = _____

Slack   = _____

D. Complete the F5 RAG Simulink Design

The direct-form FIR filter can be optimized in several ways. First, we can use a constant coefficient multiplier block (called gain) instead of the general-purpose multiplier. Or, we could use the transposed FIR form to reduce the adder delay. Another way would be to combine the coefficients using the reduced adder graph (RAG) you developed in the pre-lab.

1. Download "**F5transposed.mdl**" from the class webpage and put the file in the **DSPwFPGAs** folder.

2. Complete the design (i.e., add your reduced adder graph) and simulate. Carefully choose the bitwidth to represent your coefficient. Use "just enough" bits for the power-of-two values otherwise the RAG will need more LCs than necessary. **Print** your design and simulation.

Lastname: _____
5Digit SS:_____

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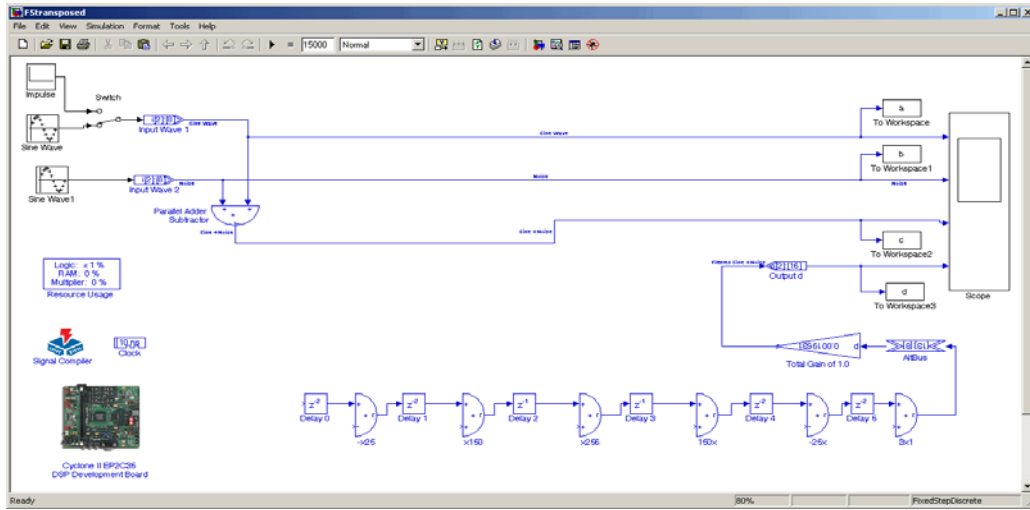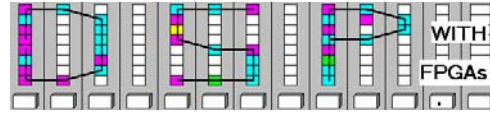**FIR Filters**

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Figure 5: F5Transposed Block SFG

3. Simulate the design in **Simulink** to verify the functionality. (**Print** scope output to turn in.)

4. Determine the number of logic elements, DSP 9x9, and the minimum slack of the device:

    Logic Cells   = _____

    DSP 18x18   =_____

    Slack   = _____

5. Compare this design with the direct form design f5direct.mdl. Determine the improvements:

    LCs Improvement =   _____(LCs)

    Slack Improvement =   _____(ns)

F. Deliverables:

1. Solve the problems of the pre-lab. (3 points).

2. Print the MDL files and the Simulink simulations from parts B-6, C-2, and D-2. (7 points).

Make sure your name and SS is on all pages you turn in!

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