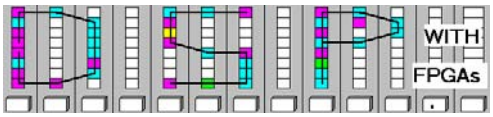
Lastname: _____

5Digit SS:_____

LABORATORY
Into. Simulink+ DSP Builder



LAB : INTRODUCTION TO SIMULINK AND DSP BUILDER
(10 points)

In this lab you will be introduced to the Simulink environment for the Cyclone II DSP Development board. In the **pre-lab** you will compute with "pencil-and-paper" the results you later expect in your design implementation. In the **design part** you will complete the design of a sine wave generator and become comfortable with the Simulink environment.

Lab Objectives

After completing this lab you should be able to

- Associate components with their library
- Understand the Simulink/DSP Builder design flow
- Design and simulate a circuit using Simulink

Pre-lab (3 points)

1. Download the board documentation for the Cyclone II DSP edition from Altera's webpage or the course webpage and answer the following questions.

   a. What is the exact name of the FPGA on the board: _____

   b. How many logic elements (LEs) has the FPGA? _____

   c. How many embedded 18x18 multipliers are in the FPGA? _____

   d. How many M4K embedded RAMs does the FPGA has ? _____

   e. What is the frequency of the FPGA on-board oscillator ? _____ MHz

   f. Determine the pin locations for LED0 =____, Global Reset (SW6)= ___, and On-board Oscillator = ___.

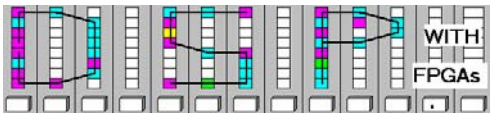
2. For the following elements determine the vendor library, library name and subgroup of the library (D2A is shown as and example):

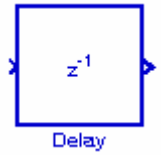
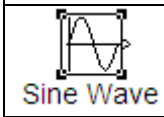
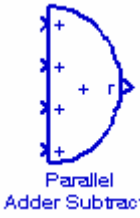
Element	Directory	Sub-directory	Sub-Sub-directory
	Altera DSP Builder Blockset	Boards	CycloneIIEP2C35
			

Lastname: _____

5Digit SS:_____

LABORATORY
Into. Simulink+ DSP Builder



3. A function generator uses a LUT to store a sine table. The input to the function generator is a triangular signal, and at the output an unsigned sine wave should be observed. The frequency of the sine wave should be 100 kHz . The triangle function is generated with an accumulator (increment *M*) running at 100 MHz and B=17 bit width.

g. Determine the period length of the 100 kHz sine wave: T = _____

h. Determine M for the 17 bit accumulator with an output frequency of 100 kHz: M = _____

4. The sine frequency is in general much too high to be seen on the 7-segment LEDs. The MSBs of an 29 bit accumulator are used for the LED display.

g. Determine the LED period length for M=1 and 29 bit accumulator:

T = _____

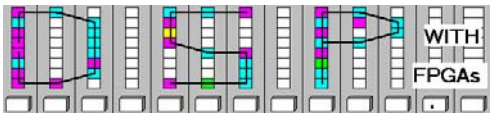
h. Determine the period for the 17 bit accumulator with M =1

T = _____

Lastname: _____

5Digit SS:_____

LABORATORY
Into. Simulink+ DSP Builder



Simulink Design-lab

Follow the directions below to implement sine wave generator circuit.

.

A. Getting Started

If you are in B114 or the digital logic lab:

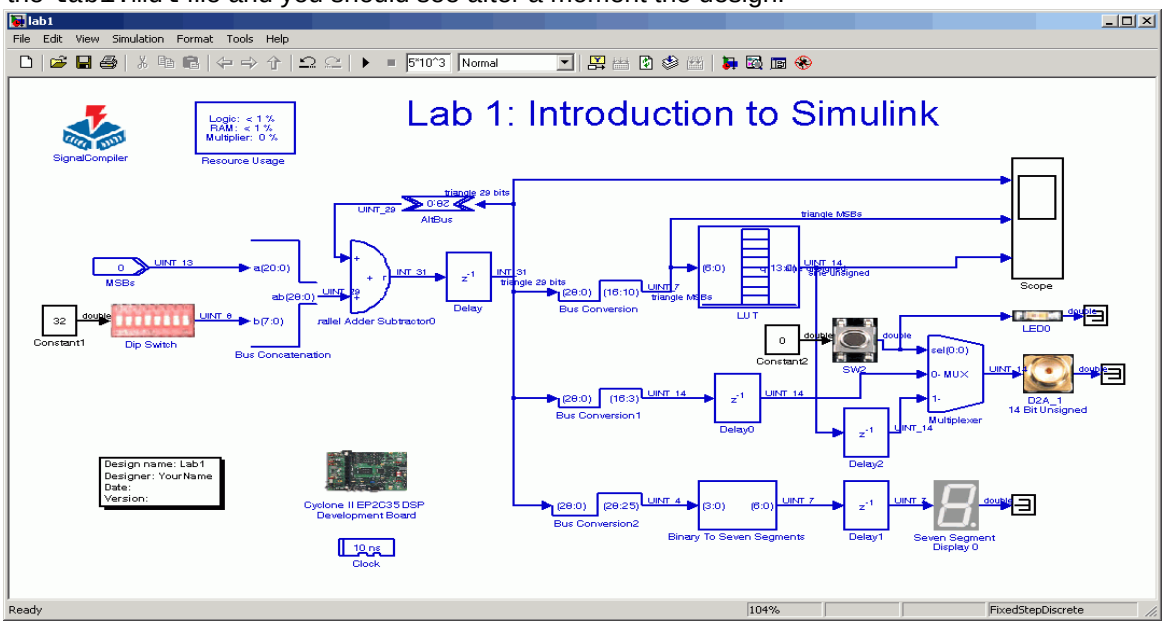
1. On the desktop double click on **Engineering folder**.
2. Double click on **MatLab** icon  to start **MatLab**.
3. From the icon list in the **MatLab** window click on the **Simulink** icon  to start **Simulink.**
4. You should not save anything on the local hard disk. You will have to use a USB stick, or your "mapped" home directory to save the files. Create a New Folder named **DSPwFPGAs** on your mapped network drive.

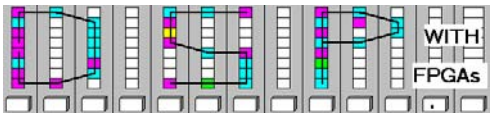
B. Compiling an Existing Design

1) Download the file `lab1.mdl` from the class webpage and put the file in the **DSPwFPGAs** folder.

2) Click on the "Current Directory" selection icon  and select as current directory the **DSPwFPGAs** folder.

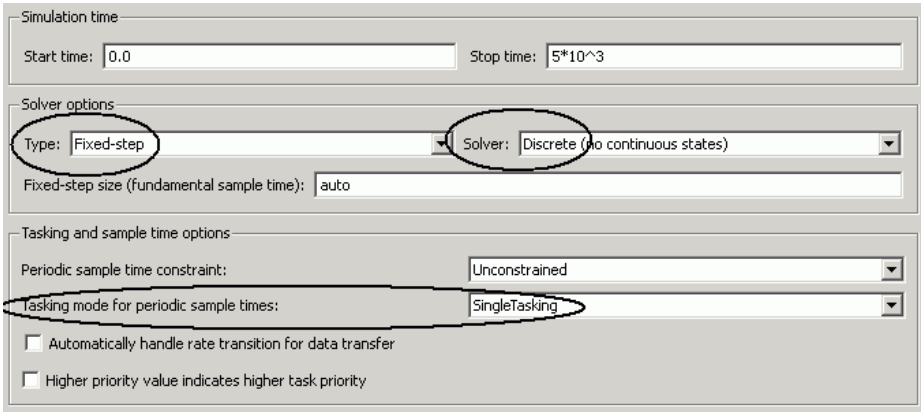
3) The files in the **DSPwFPGAs** folder are now visible in the upper left **MatLab** window. Double click on the `lab1.mdl` file and you should see after a moment the design:





4) Run the Simulation by either pressing the  icon, hitting **Ctrl+T**, or selection **Start** in the Simulation menu. On the menu bar, go to **Simulation** and click on **Configuration Parameters,** or use **CTRL+E**. Choose the following configuration parameters:

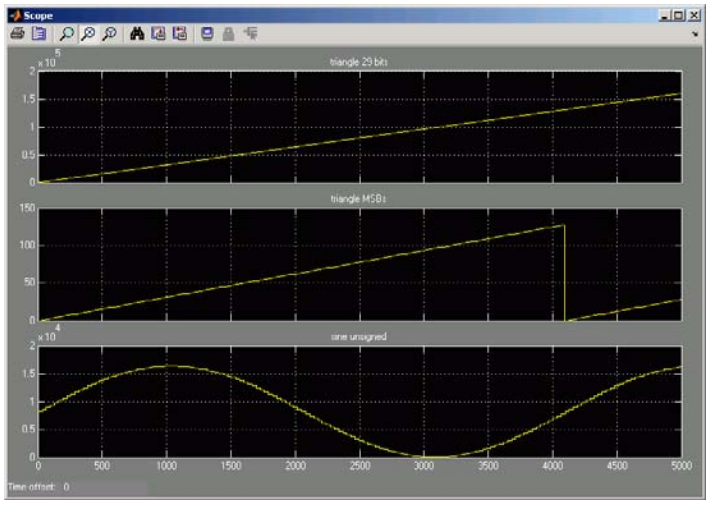
Type: Fixed-step
Solver: discrete (no continuous states)
Tasking mode for periodic sample times: single tasking

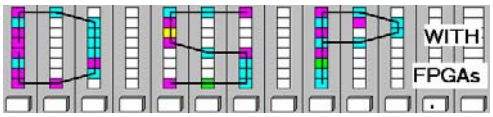


5) On the menu bar, go to **Format**, **Port/Signal Display**. Make sure **Port Data Types** is checked. This way, Simulink will show the data types leaving each block. This can be very useful when "debugging" a larger design.

6) To simulate the design, click on the **Start Simulation** button  , choose **Start** under the **Simulation** menu, or use **CTRL+T**.

7) In order to see the output of the simulated scope double-click on the **Scope** block. A window should appear with three graphs, one for each input. Click the  icon to Auto scale all the graphs. The result should be similar to the following figure.

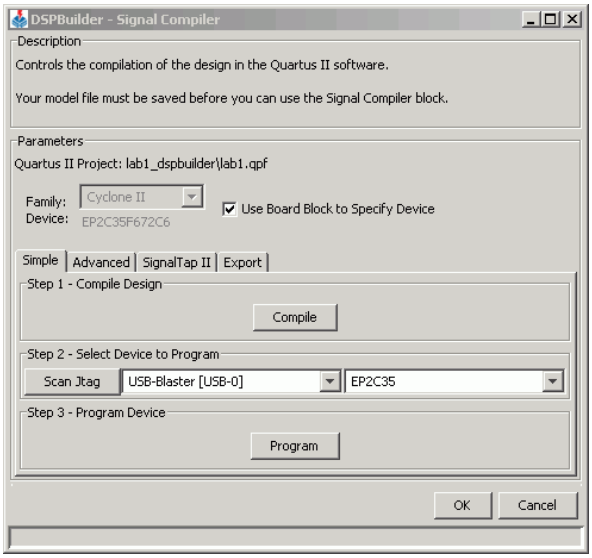




8) Next double-click the **SignalCompiler** block. Note That you can only compile the design on a PC that has a DSP Builder license enabled.

9) Check the box for **Use Board Block to Specify Device** if you have a computer with board, otherwise use **Family: Cyclone II** and **Device:EP2C35F672C6**. For step 1 select **Simple** Compile option and then click **Compile**.

10) The compile is down when the "wiper" in the bottom window disappears. Click on the **Scan Jtag** button and then select the **USB-Blaster** and **EP2C35** option, see figure below.



7) Double click the **Resource Usage** block and determine the following data:

lab1/Resources

Logic Cells = _____

M4Ks = _____

DSP 18x18 = _____

lab1/Timing

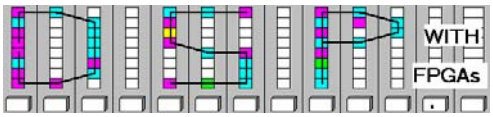
Minimum Slack = _____ (ns)

Source = _____

Destination =_____

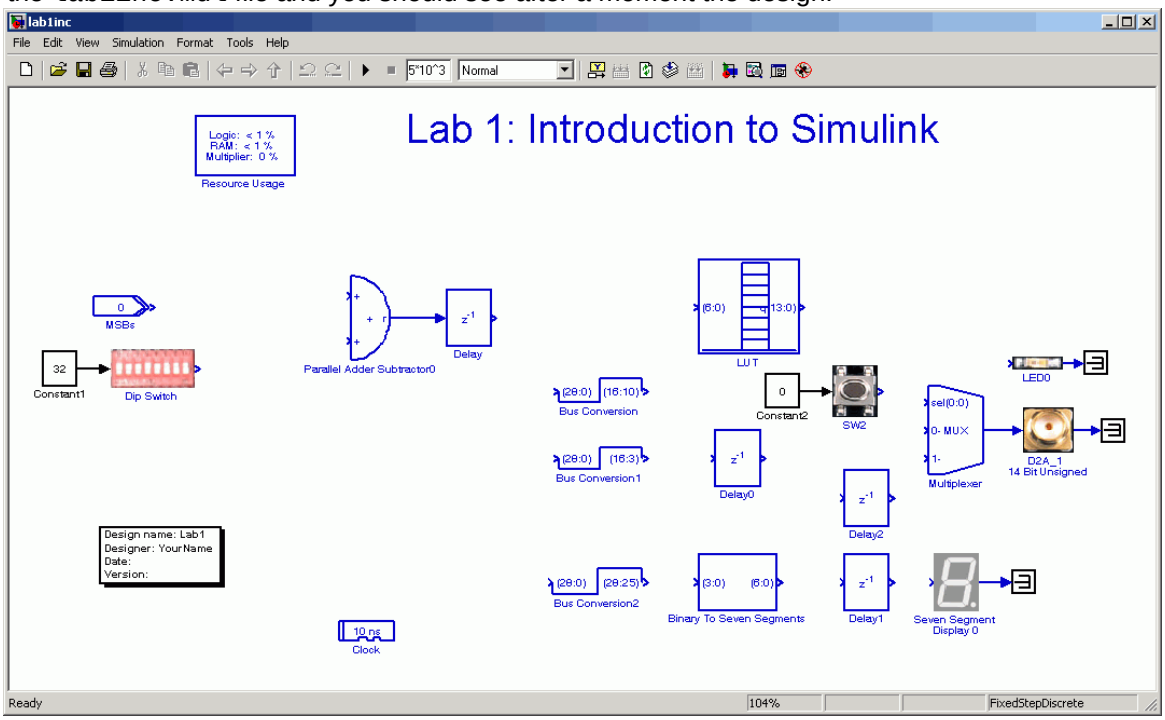
C. Completing The Simulink Design

1) Download the file `lab1inc.mdl` from the class webpage and put the file in the **DSPwFPGAs** folder.



2) Click on the "Current Directory" selection icon  and select as current directory the **DSPwFPGAs** folder.

3) The files in the **DSPwFPGAs** folder are now visible in the upper left **MatLab** window. Double click on the `lab1inc.mdl` file and you should see after a moment the design:

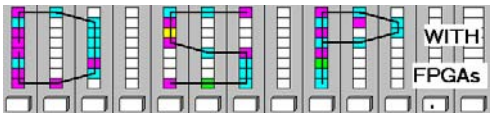


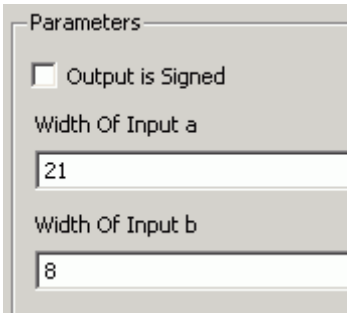
4) Begin completing the circuit diagram by adding the **SignalCompiler** and the **Cyclone II EP2C35 DSP Board configuration**.

   a. Open the Library Browser icon  and select the **Altera DSP Builder Blockset** directory.
   b. Select the **AltLab** subdirectory and find the **SignalCompiler**.
   c. Drag the **SignalCompiler** block from the library window to your diagram.
   d. Select the **Boards->CycloneIIEP2C35** subdirectory from the **Altera DSP Builder Blockset** directory.
   e. Left-click and drag the **Altera Cyclone II EP2C35 DSP Development Board** block to your diagram.

5) Add and connect the **Bus Concatenation** block.

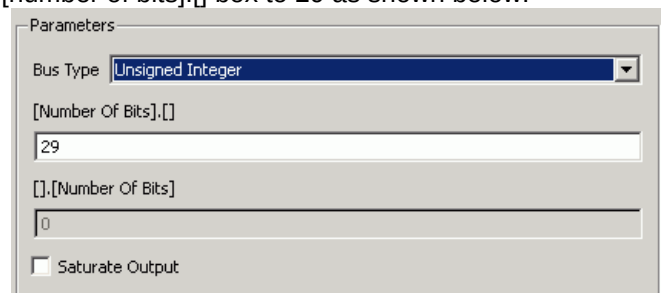
   a. Find the **Bus Concatenation** block in the **IO & Bus** subdirectory.
   b. Left-click and drag the block to the diagram.
   c. Double-click the block to view the settings and adjust them as shown below.



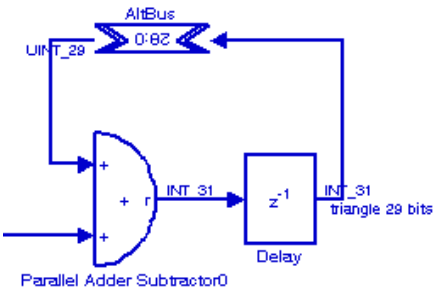


d. Click **OK** to save the parameters.
e. Left-click the MSBs **Input** block, hold the **Ctrl** key, left-click on the **BusConcatenation** block, and release the **Ctrl** key. (Notice how the connection between the **Input** block and the **BusConcatenation** block is made)
f. Left-click the **Dip Switch** block, hold the **Ctrl** key, left-click on the **BusConcatenation** block, and release the **Ctrl** key.
g. Connect the **BusConcatenation** block to the **Parallel Adder Subtractor** by dragging the output arrow from the **BusConcatenation** block to the lower input of the **Parallel Adder Subtractor**. (Notice how this method can also create connections between blocks)

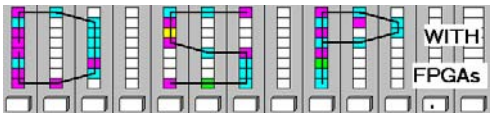
6) Connect the input and output signals for the **Parallel Adder Subtractor**.
   a. Find the **AltBus** block in the **IO & Bus** subdirectory.
   b. Rotate the block twice so that it is pointing opposite the natural direction by either hitting **Ctrl+R**, going to **Format -> Rotate Block** on the toolbar or after right clicking the block.
   c. Place the block on the diagram and double-click the block to view the settings.
   d. Change the [number of bits].[] box to 29 as shown below:



   e. Click **OK**, left-click the **AltBus** block and connect it to the top input of the **Parallel Adder Subtractor**.
   f. Left-click the **Accumulator** block and connect it to the input of the **AltBus** to look like:



7) Connect all the blocks that are floating.
   a. Start by connecting each of the **BusConcatenation** blocks to the block immediately to its right using either method described if previous steps.



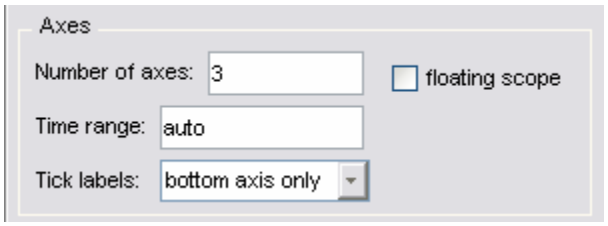
b. Left-click the input ports for each block and drag a wire to connect to the wire exiting the **Parallel Adder Subtractor**.
c. Now all three **BusConcatenation** blocks should be connect to the output of the **Delay** block right to the **Parallel Adder Subtractor** and whatever block is on its right.
d. Left-click the **Binary To Seven Segments** at the bottom right of the diagram and connect it to the **Delay 1** and then the **Delay 1** to the **Seven Segment Display 0** block.
e. Left-click the **LUT** and connect it to **Delay 2** block to its bottom right, then connect the **Delay 2** to the 1 input to the **2-to-1 Multiplexer** block.
f. Left-click the remaining disconnect **Delay 0** block and connect it to the 0 input of the **2-to-1 Multiplexer** block.
g. Connect the **SW2** block to the sel[0:0] input on the **n-to-1 Multiplexer** and to the **LED0**. Connect the **2-to-1 Multiplexer** block to the **D2A_1 14 Bit Unsigned** block.

8) Now there is a working version that can be downloaded to the development board that should look like the `lab1.mdl` design.

D. Simulating your design in Simulink

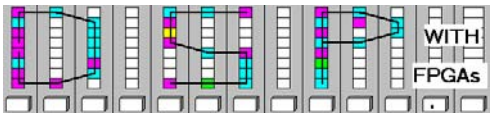
As you might have noticed from part B, the steps to actually downloading the model to the board take a lot of time. So it is often the case that you'll want to see the output of the schematic without downloading it to the board. In this case, a scope will be used to view the output at particular points of the schematic.

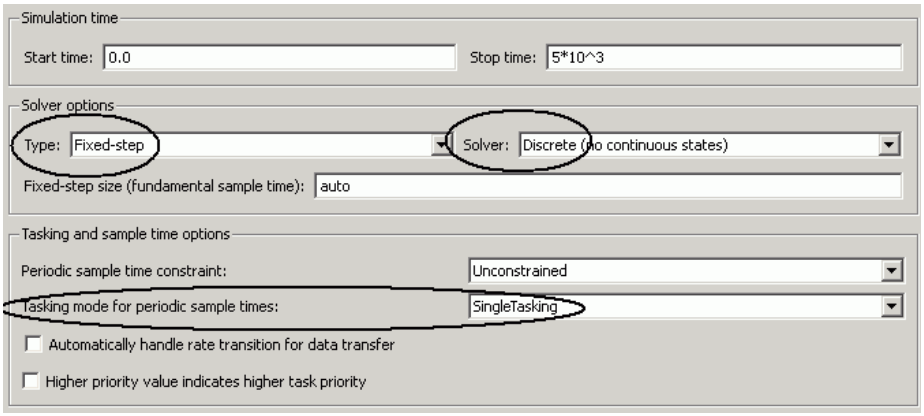
1. Add the **Scope** to the schematic.
   a. To add a scope, open the Library Browser by clicking on the  icon.
   b. Find the scope in directory found in the pre-lab.
   c. Drag the **Scope** block to the diagram and place it in the top right corner of the window.
   d. Double-click the **Scope** block to have the graph window pop up.
   e. Click the Parameters icon  .
   f. Change the number of axes to 3 as shown below:

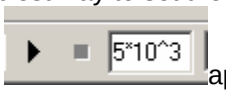


   g. Click OK and return to the diagram. You should see three inputs into the **Scope**.
   h. Click on the top input to the **Scope** and draw a wire to the connection from the input of the 29 bit **AltBus**.
   i. Click on the middle input to the **Scope** and draw a wire to the connection between the **BusConcatenation** block and the **LUT**.
   j. Click on the bottom input to the **Scope** and draw a wire to the connection at the output of the **LUT**.

2. Set the Simulation configuration parameters and stop time to 5000.
   a. Select **Configurations Parameters** from the **Simulation** menu from the toolbar in the **Simulink** window (or hit **Ctrl+E**). You should see the frame below in the window that appears.





b. Change the Type to be **Fixed-step** and Solver should be set to **discrete (no continuous states)**.
c. Change the Stop time to read 5000 or 5*10^3. Click OK and the **Simulink** window should show the stop time as seen in (d).
d. The simplest way to set the simulation stop time is to change the value in the **Simulink** window, 

appropriately.

3. Run the Simulation by either hitting the  icon, hitting **Ctrl+T**, or selection **Start** in the Simulation menu.

4. Double-click the **Scope** block and the graph window with three graphs should appear. Hit the  icon to Auto scale all the graphs. Verify that you get two triangle and a sin function as in part B.

E. Compiling Your Design using SignalCompiler

Complete steps 4 – 6 from part B where the LSBs **Input** block is equal to the value M you computed in the Prelab for an output 100 kHz frequency.

From the **Resource Usage** block or the report file determine the following data:

Logic Cells = _____
Minimum Slack = _____ (ns)

Hint: If Slack is not displayed in MDL; use `lab1.sta.rpt` from the `lab1_dspbuilder` folder instead. Look for `Slow Model Setup: 'Clock'`

F. Download your design to the FPGA board

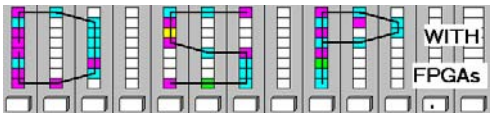
Once you have completed compiling your model, you can now download it to the board.

1. If no DSP board is at your workbench move to one that does.

2. Power up the board if needed by plugging it in and flipping the switch next to the power supply port so that the blue LED is lit.

3. Once the compilation steps are done, the **Program** button can be used. If not, check the design for error and re-run the compilation steps.

G. Observing the Board



1. The switches form an eight bit input, which corresponds to the value *M* calculated for the prelab. Observe how changing the value of the input affects the speed of the seven segment display.

2. Turn on the oscilloscope. One channel will display the sine wave through the digital to analog converter. Pressing SW2 will display the output of the accumulator sliced to it's most significant bits and put through the digital to analog converter.

3. Determine the period length and frequency ($F=M/2^{17}*F_{in}$) of the sine wave for:

   M=64 T = _____ F= _____

   M=131 T= _____ F= _____

   M=255 T= _____ F= _____

4. Show your working FPGA board design to the lab instructor.

H. Deliverables

1) Solve the problems of the pre-lab. (3 points).

2) Print the completed schematic for the MDF file `lab1inc.mdl` and the Simulink simulation scope plot (7 points).

Make sure your name and SS is on all pages you turn in!