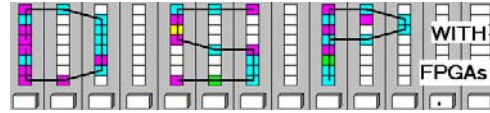


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LAB SFG: INTRODUCTION TO SIGNAL FLOW GRAPHS
(10 points)

In this lab you will be introduced to signal flow graphs (SFG), system analysis and synthesis. DSP systems can be described by different methods. Most frequently used are the differential equation, the **z**-transform, and the SFG. When designing a system, the analysis of the properties of the system also plays an important role.

In the **pre-lab** you will compute with “pencil-and-paper” the results you later expect in your design implementation. In the **design part** you will design three systems and analyze their response to an impulse sequence.

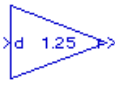



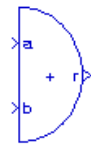
Lab Objectives

After completing this lab you should be able to

- Characterize systems by linearity, stability, causality and time invariance
- Understand the difference between FIR and IIR systems
- Design and simulate nonlinear, FIR and IIR systems using Simulink

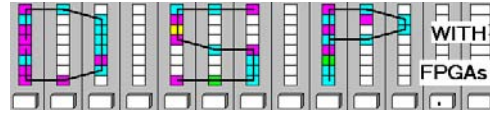
Pre-lab (5 points)

1. SFG are built using basic building blocks. Give a short description and the corresponding difference equation for the 5 blocks below. The gain block is given as an example. Use $a[n]$ and $b[n]$ as inputs and $y[n]$ as output.

Element	Short description	Differential equation
 Block 1	Scaling with a constant value of 1.25	$y(n) = 1.25 * a(n)$
 Block 2		
 Block 3		
 Block 4		
 Block 5		

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- For each of the three systems shown below, determine the response to the two-impulse sequence shown in figure 2 (amplitudes are +10 and -20). Note that the pattern block of system 1 produces a repeating length-two sequence of 1's and 0's.

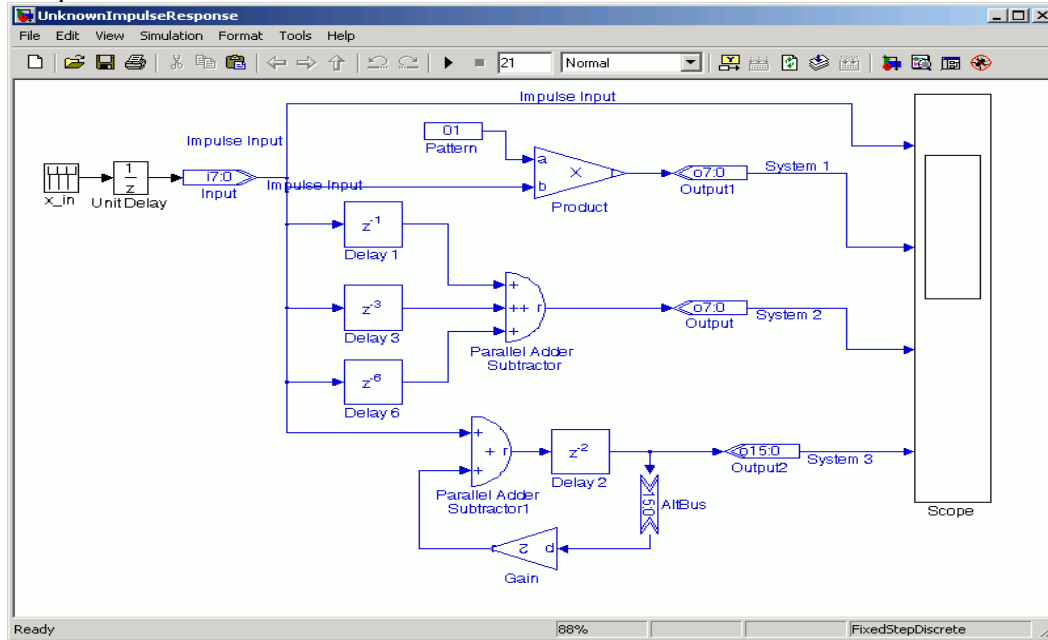


Fig. 1: Three systems with unknown impulse response.

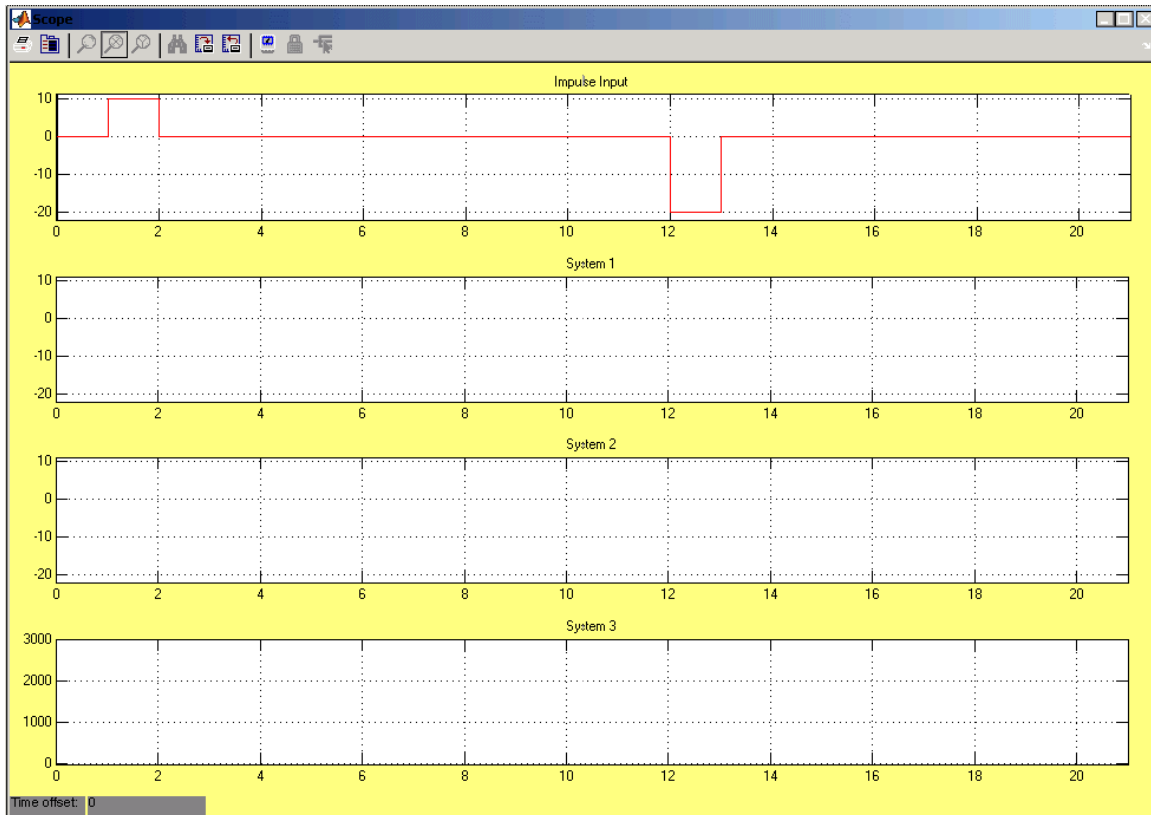
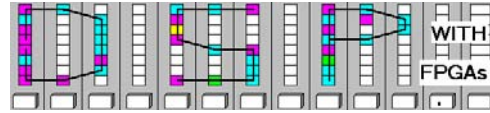


Fig. 2: Scope plot for the three unknown impulse responses.

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3. The following figure shows three black box systems. The SFG of the each system is unknown, but their responses to an impulse sequence of +10 and -20 have been measured and are shown in Figure 4. Use the given impulse responses to determine the difference equations of the systems, and then fill in the missing SFGs in Figure 3.

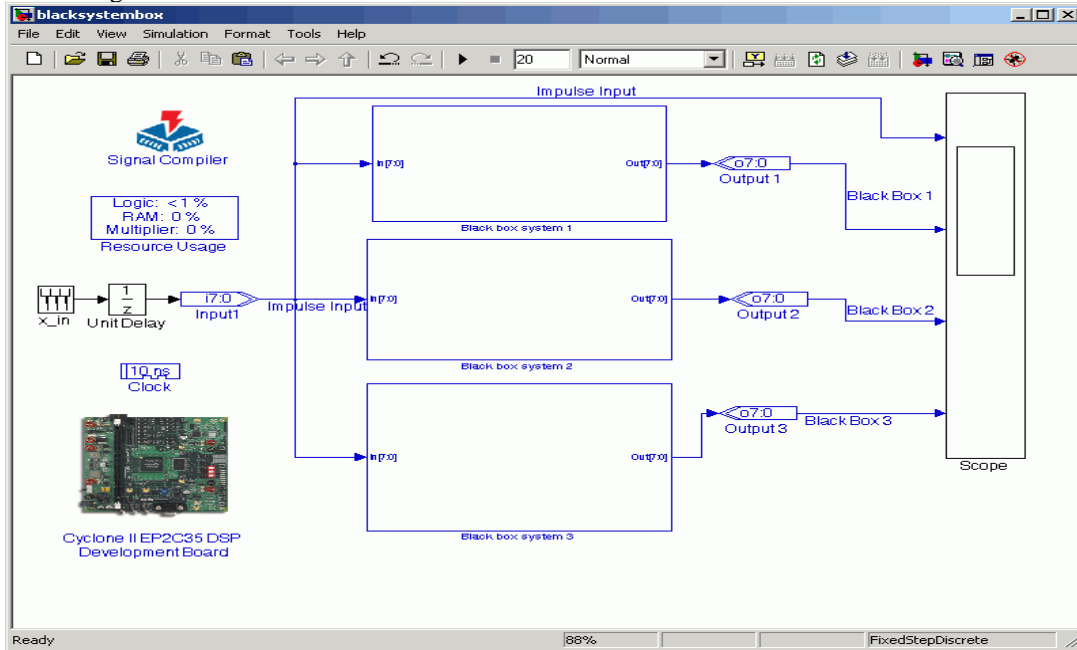


Fig. 3: Black box systems with known impulse responses.

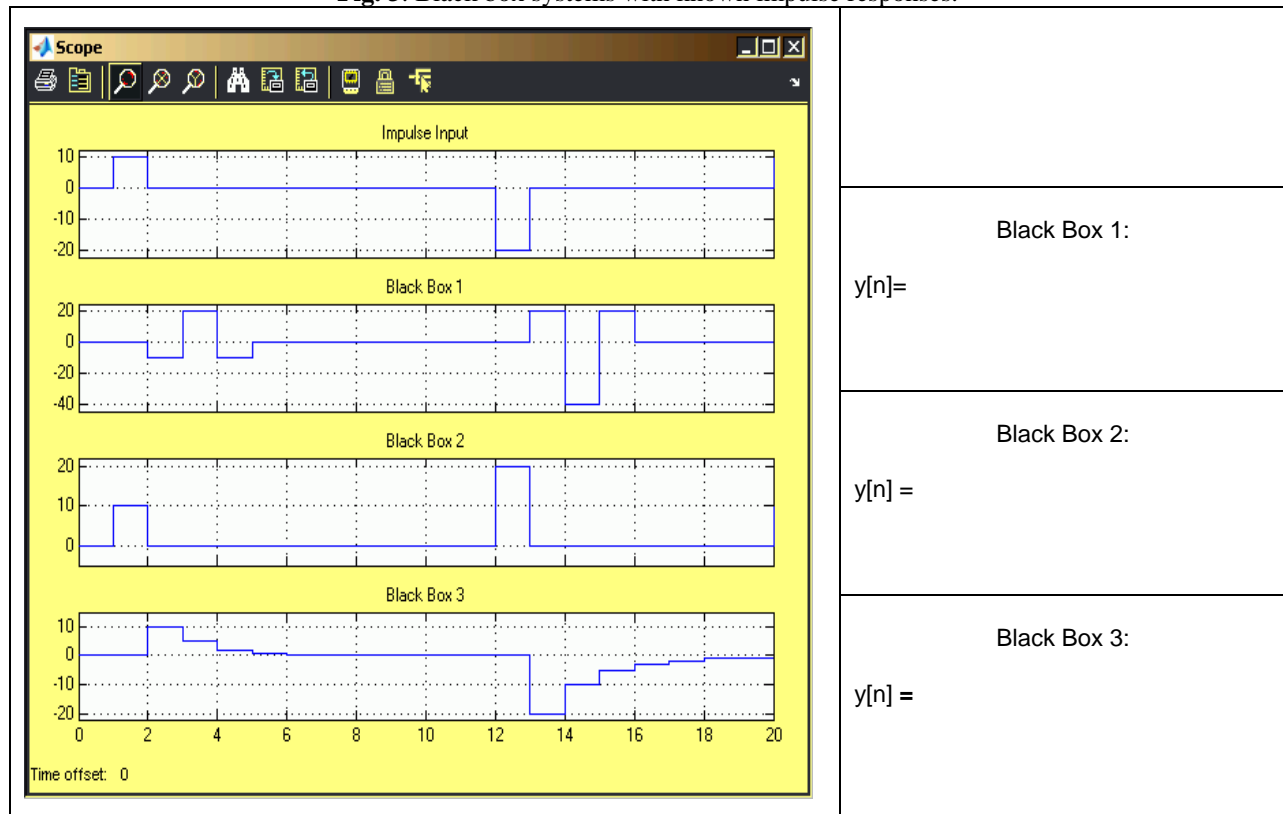
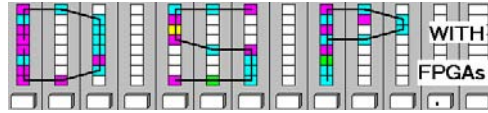


Fig. 4: Black box system measured responses to two impulse of 10 and -20.

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Simulink Design-lab


Follow the directions below to implement the circuit shown in Fig. 3.

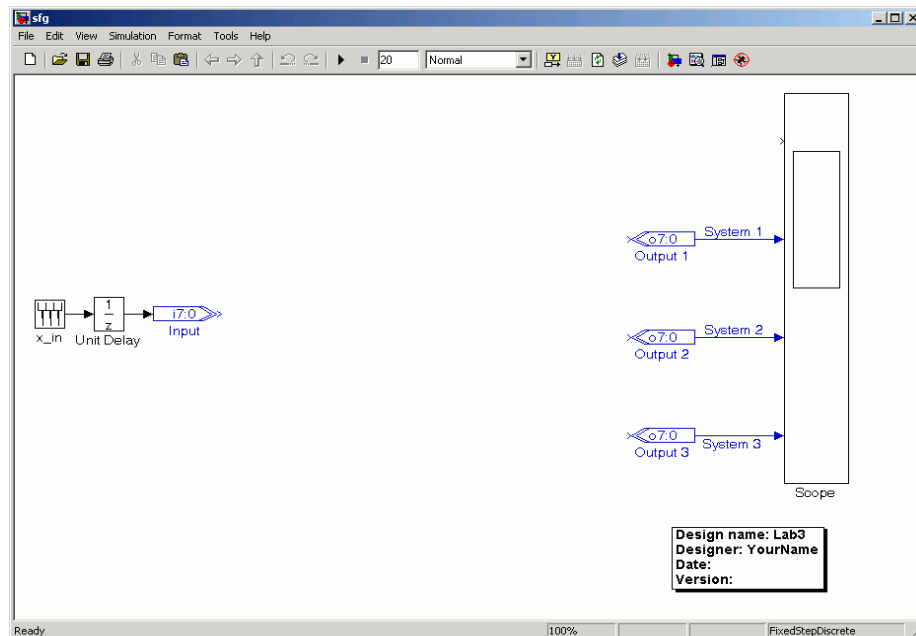
A. Getting Started

If you are in B114 or the digital logic lab:

1. On the desktop double click on **Engineering folder**.
2. Double click on **MatLab** icon  to start **MatLab**.
3. From the top icon list in the **MatLab** window click on the **Simulink** icon  to start **Simulink**.
4. You should not save anything on the local hard disk. You will have to use your own Zip, floppy disk, USB flash drive, or your "mapped" home directory to save the files. Create a New Folder named DSPwFPGAs on your mapped network drive..

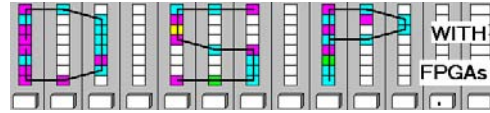
B. Design the SFG systems

1. Download the file `sfg.mdl` from the class webpage and put the file in the **DSPwFPGAs** folder.
2. On the **MatLab** toolbar, click on the "browse for folder" icon  and select your **DSPwFPGAs** folder as the new directory.
3. The files in the **DSPwFPGAs** folder are now visible in the upper left **MatLab** window. Double click on the `sfg.mdl` file and after a moment you should see the incomplete design:




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C. Completion of the MDF design

1. Complete your design using the signal flow graph you developed in the pre-lab for the black-box system. Use elements from the Altera DSP Builder Blockset (found in the **Simulink** library browser ).
2. Verify your design via a **Simulink** simulation. Make sure the impulse responses match those from part 3 of the pre-lab! Set the correct simulation parameters by clicking "Simulation" on the **Simulink** toolbar and then "Configuration Parameters." Match the solver settings to those in the following window:

Simulation time
Start time: 0.0 Stop time: 20

Solver options
Type: Fixed-step Solver: Discrete (no continuous states)
Fixed-step size (fundamental sample time): auto

Tasking and sample time options
Periodic sample time constraint: Unconstrained
Tasking mode for periodic sample times: SingleTasking

3. Add blocks for **Resource Usage**, a 10 ns **Clock** block, **CycloneII EP2C35** board, and **Signal Compiler**. Then Compile the design using **Signal Compiler** and determine using the Quartus report files or the **Resource Usage** block

Resources: Logic Cells = _____

Timing: Slack = _____

4. Finally, complete the author field for Lab 3.

F. Deliverables:

1. Solve the problems of the pre-lab. (5 points).
2. Print the MDF schematics file and the correct Simulink simulation plots (5 points).

Make sure your name and SS is on all pages you turn in!