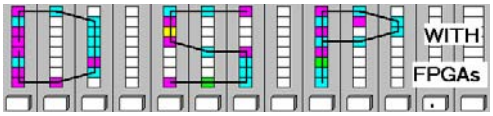
Lastname: _____

5Digit SS:_____

**LABORATORY**
**Signal + Systems**




## LAB S+S: SIGNAL AND SYSTEMS
## (10 points)

In this lab you will be introduced to signal and system design, system analysis and synthesis. DSP systems can be described by different methods. Most frequently used are the difference equation, the ***z***-transform, and the signal flow graph circuit. When designing a system, the analysis of the properties of the system also plays an important role.
In the **pre-lab** you will compute with "pencil-and-paper" the results you later expect in your design implementation. In the **design part** you will design three systems and analyze their response to an impulse sequence.

## Lab Objectives

After completing this lab you should be able to

- Characterize systems by linearity, stability, FIR and IIR behavior
- Understand the difference between FIR and IIR systems
- Design and simulate nonlinear, FIR and IIR systems using VHDL in Quartus II

## Pre-lab (5 points)

1. Below you find the VHDL code of three systems a, b, and c. Determine the RTL view of the 3 systems, the difference equation for each system, and the system properties.

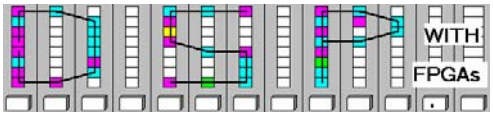
```
1  PACKAGE b_bit_int IS    -- User defined types
2    SUBTYPE WORD IS INTEGER RANGE -2**15 TO 2**15-1;
3    TYPE ARRAY_WORD IS ARRAY (1 TO 4) OF WORD;
4  END b_bit_int;
5
6  LIBRARY work; USE work.b_bit_int.ALL;
7
8  LIBRARY ieee; USE ieee.std_logic_1164.ALL;
9  USE ieee.std_logic_arith.ALL;
10 ---------------------------------------------------
11 ENTITY ude IS
12   PORT (clk : IN  STD_LOGIC;
13         two : IN WORD := 2;
14         x   : IN  WORD; -- input to all three systems
15         y_a : OUT WORD; -- Output to first system (a)
16         y_b : OUT WORD; -- Output to second system (b)
17         y_c : OUT WORD); -- Output to third system (c)
18 END;
19 ---------------------------------------------------
20 ARCHITECTURE fpga OF ude IS
21   SIGNAL x_n : ARRAY_WORD := (0,0,0,0); -- Delay Array
22   SIGNAL u, v : WORD := 0; -- WORDs
23   SIGNAL cnt : INTEGER RANGE 0 TO 3 := 0;
```

Lastname: _____

5Digit SS:_____

**LABORATORY**
**Signal + Systems**




```
25  BEGIN
26    P1: PROCESS     -- Implement the registers
27    BEGIN
28      WAIT UNTIL clk = '1';
29      x_n(1) <= x;
30      FOR i IN 1 TO 3 LOOP -- Input delay line
31        x_n(i+1) <= x_n(i);
32      END LOOP;
33      v <= x + two * u;
34      u <= v;
35    END PROCESS;
36
37    y_a <= x + x_n(2) + x_n(3);
38    y_b <= x ** 3;
39    y_c <= u;
40  END fpga;
```

**Fig. 1**: VHDL code of 3 system a, b and c.

Provide the RTL view of the systems:

| | |
|---|---|
| **y_a** | |
| **y_b** | |
| **y_c** | |

Characterize the systems:

| **System:** | **(a)** | **(b)** | **(c)** |
|---|---|---|---|
| ***y*[*n*]=** | | | |
| **FIR/IIR** | | | |
| **Stable** | | | |
| **Linear** | | | |

2. The following figure shows the simulation result of three black box systems. The RTL viewer circuit and difference equation of each system is unknown, but their responses to an impulse sequence of +10 and -20 have been measured. Use the given impulse responses to determine the difference equations of the systems and then fill in the missing RTL viewer circuit (using adders, registers, and multipliers) in Figure 3.

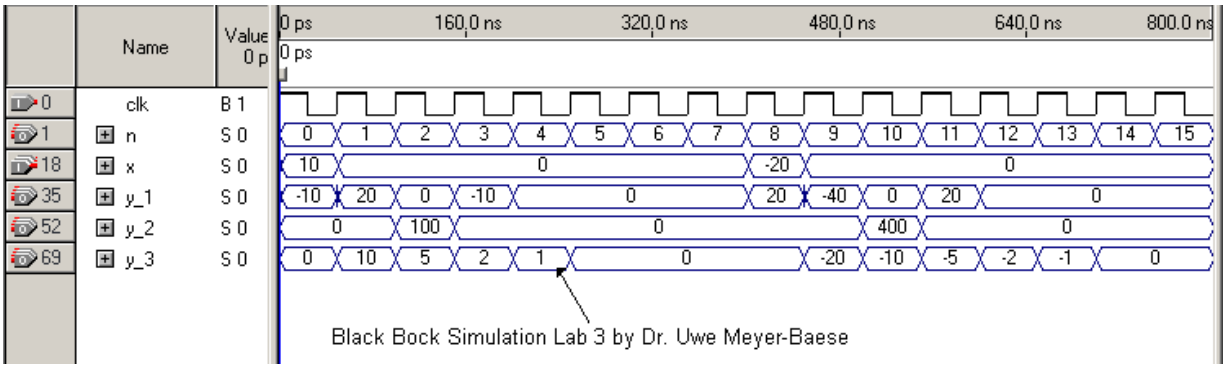
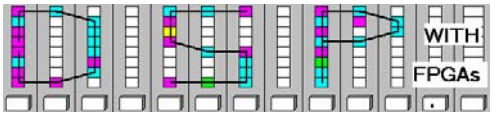



**Fig. 2**: Black box system responses to two impulses of 10 and -20.

| | |
|---|---|
| **Difference Equation 1:** | ***y*[*n*]=** |
| **RTL View System 1:** | |
| **Difference Equation 2:** | ***y*[*n*]=** |
| **RTL View System 2:** | |
| **Difference Equation 3:** | ***y*[*n*]=** |
| **RTL View System 3:** | |

**Fig. 3**: Black box systems with known impulse responses.
(Hint: System 1 has FIR, System 2 is nonlinear, and system 3 has IIR.




## VHDL Design-lab

Follow the instruction below to complete the design of the three black box systems.

### A. VHDL Coding of the 3 Black Box Systems

When implementing the black box system 1-3 (introduced in prelab part 2) use the following recommendations:

1. Start with a header and a brief description including the difference equations of the three systems. To simplify the design use a single VHDL file, NOT three components.

2. Data types: Use binary STD_LOGIC for clock `clk` and a 16 bit signed integer type for all other data including the I/O ports `n`, `y_1`, `y_2`, and `y_3`.

3. Match the simulation shown for the three systems in the prelab by following the usual method learned in lab 1+2.

### B. Deliverables:

1. Solve the problems of the pre-lab. (5 points).

2. Print the VHDL file and the correct VWF simulation including e-signature (5 points).

**Make sure your name and SS is on all pages you turn in!**