

Errata 4th edition

for the book

Digital Signal Processing with Field Programmable Gate Arrays

by

Dr. Uwe Meyer-Baese

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EMAIL :

Uwe.Meyer-Baese@ieee.org

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Chapter 2:

Page 150 line 5 from bottom: replace (2.67) with (2.64)

Chapter 3:

Page 223 Exercise 3.20(g) second line: replace (a)-(g) with (a)-(f)

Chapter 4:

Page 242 before VHDL code: Remove (4.15), and add:

Note that the HDL implementation is not a verbatim design of Fig. 4.14. It has the same non-zero poles/zeros as we can see from the impulse response but has addition delay in the x path such that a register is placed after each adder.

Page 292 Fig. 4.56 Labels: 1. AP top left: replace “c” with “c1”

2. AP top right: replace “L3” with “I2” and replace “c1” with “c2”

3. AP lower left: replace “L1” with “I3” replace “C2” with “c2”

Page 302 Exercise 4.9: replace `csd3e.exe` with `csd.exe`

Page 302 Exercise 4.10a: replace “form II” with “form I”

Chapter 5:

Page 312/3 VHDL comments: Replace “m[0]= 127” with “m[0]=124” and “g[0]=127” with “g[0]=124”

Page 378 Fig. 5.62: switch outputs “G(z)” and “H(z)”

Page 388 Example 5.23: add factor k to g[n] and add factor 1/k to h[n]

Page 413 Exercise 5.14: replace `csd3e.exe` with `csd.exe`

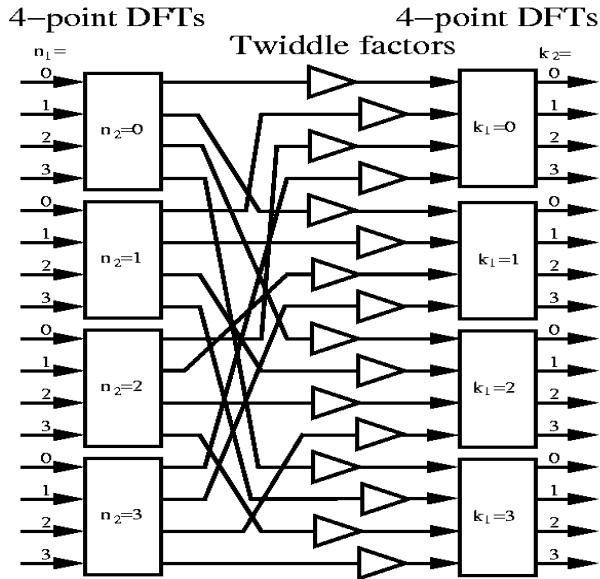
Chapter 6:

Page 430 VHDL code: Replace “unsigned” with “signed”

Page 435 Fig. 6.11: switch inputs x[2] and x[4]

Page 443/444/448 Fig. 6.15, 6.16 and 6.17: Replace “dif256” with “fft256”; same in `fft256.do` on CD

Page 467 Fig. 6.25 needs to be replaced with the following figure:



Page 469 Exercise 6.17: replace “ $y = [x(1:2:N); x(N:-2:2)];$ ” with “ $y = [x(1:2:N), x(N:-2:2)];$ ”

Chapter 7:

Page 520 Table 7.15: Replace “1,0” with “1.0” and “1,5” with “1.5”

Chapter 8:

Page 540 third equation from bottom: Remove (

Page 543 last equation: add = after r_{dx}

Chapter 9:

Page 663 Table last row: replace $[^a-b]$ with $[^a-c]$

Page 737 Table second line from bottom: replace E2AA with E2AB

Chapter 10:

Page 773 line 2: replace $N(N+1)/2$ with $N(N-1)/2$

Page 773 line 2: replace 2^N with N

Page 773 line 4: replace $N+1$ by N .

Page 774 Fig. 10.16(a) add final stage sorting network for Minimum/Maximum computation.

Page 793 Exercise 10.14: replace 2×2 by 3×3 .

Page 794 Exercise 10.18: replace S&H by S&P.