

# Xilinx HDL Manual 4/e

by

# Dr. Uwe Meyer-Baese

Book Webpage: http://www.eng.fsu.edu/~umb Please report bugs to the author's email : <u>Uwe.Meyer-Baese@ieee.org</u>

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This manual contains the simulation for ModelSim, ISE and Vivado coding in HDL when using Xilinx tools of the 4. Edition book *Digital Signal Processing with Field Programmable Gate Arrays*, published by Springer Verlag, Heidelberg.

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## **The Xilinx HDL Manual**

Field-programmable gate arrays (FPGAs) are revolutionizing digital signal processing. Many front-end digital signal processing (DSP) algorithms, such as FFTs, multi channel filter banks, or wavelets, to name just a few, previously built with ASICs or programmable digital signal processors, are now most often replaced by FPGAs. The two FPGA market leaders (Altera and Xilinx) both report revenues greater than \$1 billion. FPGAs have enjoyed steady growth of more than 20% in the last decade, outperforming ASICs and programmable digital signal processors (PDSPs) by 10%.

Design of current DSP applications using state-of-the art multi-million gates devices requires a broad foundation of the engineering skills ranging from knowledge of hardware-efficient DSP algorithms to CAD design tools. This has been the foundation for the book Digital Signal Processing with Field Programmable Gate Arrays now available in the 4. Edition [1] that was mainly based on Altera's Quartus software and ModelSim simulation via "do" files.

While the design flows for Altera and Xilinx tools are similar there has been some notable difference over the years. Most visible in the handling of the simulation of the designs. We have seen the two FPGA market leaders take opposite directions in recent years. In the past Altera favored the internal VWF waveform simulator (up to Quartus II version 9.1) and now recommends the external ModelSim-Altera or Qsim. Xilinx on the other hand, since version 12.3 (end of 2010), no longer provides a free ModelSim simulator and instead provides a free embedded ISIM simulator that is integrated within the ISE Tool and the Vivado tool has a similar internal simulator called XSIM too. The two main obvious differences are that the ISIM simulator has the option to do a simulation via TCL script, while the XSIM simulator has an analog (aka waveform) display option. The simulator considerations for ISIM and Vivado is discussed later in more detail in section 0.2.

The Altera Quartus II software comes with two free simulator options. The ModelSim-Altera allows us to use the professional tool from Mentor Graphic Inc. The second alterative is the Altera Qsim tool that may have a few less feature than ModelSim (e.g., no analog waveform) but is also a little easier to handle since is does not require one to write HDL test benches or DO file scripts to assign I/O signals. However, at the time of writing of the book [1] the Qsim in 12.1 did not support the Cyclone IV devices and therefore the ModelSim-Altera was selected as default simulator. Moving between VHDL and Verilog stimuli file and Altera and Xilinx was also simplified by using ModelSim-Altera DO files and not HDL test benches.

#### **0.1 Selecting the Target Platform**

If we like to select an appropriate Xilinx FPGA platform for *all* designs, then we need to provide enough resources (LE, embedded multipliers, Block RAMs, and number of pins) to host the largest designs. On the other side we may want to select a (low cost) board that is available through Xilinx University program (ZedBoard, Zybo, Nexys 4, Basys, or Atlys as of 7/2015) which are designed by Digilent Inc. and are provided at low cost even for non-university customers. Another goal maybe to use boards that are supported by the Vivado web edition software. As of 7/2015 the ZedBoard, Zynq and an Artix-7 board are supported in the Vivado web edition. Table 0.1 gives an overview of some popular boards.

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Board	Device	Avail. I/O	LUT	DSP	BRAMs
ZYBO	xc7z010t-1clg400	100	17,600	80	60
ZedBoard	xc7z020clg484-1	200	53,200	220	140
Artix-7	xc7a200tfbg676-2	400	134,600	740	365
Kintex-7	xc7k325ffg900-2	500	203,800	840	1335
Virtex-7	xc7vx485ffg1761-2	700	303,600	2800	3090

**Table 0.1:** Overview of popular Xilinx boards, their FPGAs and resources.

The maximum values for all Altera DE2 examples in [1] were 33,926 LEs, 184 multipliers 9x9, 2 Block RAMs, and 413 pins. There are only 4 designs with more than 200 pins, and many of the I/Os have been used for monitoring and placed in the I/O section to guarantee that this signals are observable. Many of these signals are not essential for the function. The fft256 design for instance has a total of 413 pins, however, essential for the function are only: clk, reset, xr\_in, xi\_in, fft\_valid, fftr and ffti, which account for 3+4x16=67 pins that would fit even on the smallest board from Table 0.1. The timing simulation will require a full compile such that all timing is available depends in part on the FPGA size. Considerable compile time can be saved (about 50%) if we use a "quick" compile strategy with less optimization as Table 0.2 shows. Compile time in general even with a big device is still reasonable for the Vivado tool.

**Table 0.2:** Compile time for a few typical boards and compile options for the fun\_text design. Synthesis alone took about 30 sec (device independent). (i7 PC; 12 GB; Win8.1;Vivado 2015.1)

Board	Option	Time
Artix Board	Standard synthesis	2:23
Artix Board	Quick flow	1:19
Zedboard	Standard synthesis	1:37
Zedboard	Quick flow	1:08
Big FPGA Xc7a2000 with 500 I/O	Quick flow	1:15
Biggest Zynq xc7z030	Quick flow	1:10

#### 0.2 Xilinx Specific HDL Design Consideration

Xilinx has announce that in the future the Vivado tool set will be supported and the ISE tool set will be retired. Unfortunately, Vivado seemed not to support any FPGA family before the 7. generation and many designer if using e.g. Virtex-6 devices will have to continue to use the ISE tools still. In the last two years since introducing the Vivado software in 2013 no effort has been seen to support older FPGA devices in Vivado. We will therefore briefly discuss the ISE simulation flow but will use whenever possible the Vivado tool in the compile file listing.

When simulating a design with the ISIM simulator we have the option to use a stimuli file from a TCL script similar to ModelSim DO files, or we can write a test bench in HDL. A test bench is a short HDL file, where we instantiate the circuit to be tested and then generate and apply our test signals with a statement like

clk <= NOT clk AFTER 5 ns;</pre>



to generate a clock with a 2 x 5ns = 10 ns clock period. However, one difficulty with the ISIM test bench comes from the fact that the circuit with timing information (i.e., \*\_timesim.vhd) is synthesized directly from the netlist and the STD\_LOGIC is used throughout the whole ENTITY description. The original ENTITY data types and GENERIC variables are ignored. If we like to use the same VHDL test bench for RTL and timing simulation then the ENTITY will be restricted to a single data type. More precise, we cannot use INTEGER, SIGNED, or FLOAT data types, and even BUFFER or GENERIC parameter would not be permitted. This can be considered a great interference with the coding for design reuse and we would need to use a separate test bench for RTL and timing simulation. However, if we do not use a test bench and simulate our circuit directly using the TCL stimuli script, then we can use the same script for RTL and timing simulation. Furthermore, for VHDL and Verilog the same stimuli file can be used; only the compile sequence will be different. The ISIM TCL scripts and ModelSim DO files are also very similar in their coding style to simplify a transition between the two simulators.

Similar restrictions apply for the Vivado XSIM simulation. Here in general a Verilog netlist on LUTbased level is used to have accurate timing simulation. Since a Verilog netlist is used even for VHDL designs a match with VHDL source code is only possible for STD\_LOGIC or STD\_LOGIC\_VECTOR and BOOLEAN type. Again we cannot use INTEGER, SIGNED, or FLOAT data types, and even BUFFER or GENERIC parameter are not be permitted. However, this applies only to the I/O interface. Within the design we can indeed use INTEGERs, and design reuse with GENERIC parameters, can be done in VHDL via CONSTANT definitions and as PARAMETER in Verilog within the designs without interference the coding requirements for the I/O ports of the designs.



Another important design consideration for the Xilinx tools is the handling of the Global set/reset (GSR) in the simulator. The idea behind the GSR is that all flip-flops in all FPGAs are set to predefined values after reset within the first 100 ns of the simulation. Only after the first 100 ns any flip-flop operation can occur. Generated timing netlist will always ensure this functionality, however, the behavior simulation does not necessary follows this by default. This is demonstrated by the function generator simulator shown in Figure 0.1 and 0.2. The function generator designed as an accumulator followed by a sine wave LUT. As can be seen in the behavior simulation (Fig. 0.1) the sine wave starts earlier than the timing simulation due to the 100 ns GSR in the timing simulation, see Fig 0.2. To avoid such a mismatch in the behavior/timing simulation it is therefore highly recommended to hold flip-flop activity via a ENABLE or RESET signal for the first 100 ns as shown in Fig. 0.3. This timing simulation can then be matched with a behavior simulation with a 100 ns reset, see Fig. 0.4.





#### **0.3 Writing Testbenches**

With today's high complex designs a substantial design effort is directed towards the verification of the circuit. As the Pentium bug in the FP divider hardware has shown us in 1995, such an insufficient testing can have a large financial impact (over \$100M for Intel) besides the image damage such a recall may have.

Verification can take many different forms. For a small design we can use the "RTL viewer" aka "System view" to inspect the synthesized circuit. For a more complicated system we may use input test stimuli generated on the fly or via a test vector look-up table generated in MatLab or with a C/C++ program. The correct output behavior can be text-based, i.e. report "mismatch" of actual and expected results, or graphical such as an oscilloscope, see Fig. 0.5.



Writing a text-based HDL testbench (TB) is not too complicated but nevertheless can be labor intensive. Until ISE 11 Xilinx offered a tool call "HDL Bencher." You had to define waveform for input signals, and you could specify or generate the desired results based on a behavior simulation. This tools is still available at www.xilinx.com/webpack/classics/wpclassic as of 7/2105, see Fig. 0.6 for an example [2]. On the other side you may have special requirements how a TB should look like and then in general it is preferred to use such a template as starting point [3]. A template typically will have the following elements:

- 1. Libraries in use such as IEEE
- 2. An "empty" entity without any ports
- 3. The "Unit Under Test" (UUT) component definition
- 4. The signals/wires/reg in use
- 5. The UUT component instantiation
- 6. Definition of period signals, e.g., clk
- 7. Definition of a-period data signals, e.g., reset, data input etc.

The Verilog TB will not have item 1 and 3. It also important to remember that the XSIM simulator orders the displayed signals by default as specified item under 4, in precisely the shown order. I.e., in order to avoid rearranging the signals in the simulator window it is recommended to sort the signals/reg/wires in the order we like to see them in the waveform window. The simulator does not care about the ordering of the components port or the order how you assign the ports in the component instantiation. Vivado Verilog and VHDL simulation will look in general very similar. Only in case we have used VHDL FSM state coding with literal names this will in Verilog be displayed as integer numbers since a literal display is not supported in Verilog simulation.

In case large input data sets are needed (e.g. designs DWTDEN, PCA, or ICA) the input data can be stored in a CONSTANT array, e.g.:

```
TYPE rom_type IS ARRAY (0 TO 1023) OF STD_LOGIC_VECTOR(15 DOWNTO 0);
CONSTANT rom : rom_type := (
X"04a9",X"0282",X"004d",X"0168",X"fd37",X"06c9",X"003c",X"0730",X"010e",X"037d",
X"fa37",X"fd32",X"04fc",X"fd72",X"024f",X"0a8f",X"0b75",X"069a",X"06eb",X"0ff0",
...
```

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In Verilog we can use a Verilog ROM definition, e.g.

```
reg [15:0] ROM [639:0];
assign data = ROM[addr];
initial begin
   ROM[0]=16'h0000;
   ROM[1]=16'h04a9;
   ROM[2]=16'h0282;
   ROM[3]=16'h004d;
...
```

Or we can take advantage of them Verilog memread function

```
initial // Data read alternative via readmem
begin
$readmemh("dcf77.mif", rom);
end
```

Of course we have to add the divider and the text by hand after we have start the Vivado behavior or timing simulation.



**Fig. 0.6:** The HDL bencher provide by ISE until version 11. (a) Testbench desired values and simulation results. (b) Error message for mismatch using ModelSim simulation at time 115 ns. Value desired was specified as decimal 50 but the simulation shows a value of decimal 51.

#### 0.4 Generating the Synthesis Data

A full set of synthesis data in general will require a device specification and a full compile that can take up substantial CPU time for a big device. The map report will show the desired values such as the number of flip-flop, LUT, I/O, Bufg, block RAMs and embedded multipliers used. Since device families have different type of logic cells, LUT and block RAM sizes this data may vary for different devices.

The ISE software will allow us to set optimization Goal to "Speed" or "Area" by a right click on "Synthesize – XST" the Process properties dialog will pop up and the -opt\_mode switch can be defined. After a full compile ISE will provide maximum clock frequency or minimum period required from the "Post-Par Static Timing Report."

The Vivado software in the "Project Manager" view will have an excellent overview of the implemented design. It will not only show the files and library used and resources in bar graph or table form, also power dissipation and timing information are shown in the "Project Summary" window, a substantial improvement to the ISE software, that has all this information too just more buried in the report files.

To get the timing data, however, Vivado has no longer the "Speed" or "Area" option as ISE, instead we need to constrain the design. The idea comes from the Synopsys ASIC constrain files, where you specify a desired clock frequency and if the synthesis reaches the clock goal, the rest of the compile effort can be directed to reducing the area of the design. At a minimum we need to specific a constrain file \*.xdc and set the clock as follows:

create\_clock -period 10 -name clk [get\_ports clk]

where clk is assumed the name of the clock signal. This will set the desired clock period to 10 ns, or 100 MHz. If that frequency is too high for the device chosen, then a negative clock skew is reported and we need to increase the period. Finding the maximum speed is therefore an iterative process, more labor intensive than with ISE. Finding a "Area" optimum is simple, we just relax the timing requirement, to say -period 1000 (i.e., 1 MHz clock) and all effort of the compiler will be used to minimize the area.

#### 0.5 Files on CD

The files on the CD include a full set of 45 VHDL and 44 Verilog projects for all examples for the book Digital Signal Processing with Field Programmable Gate Arrays from the 4. Edition [1]. Each of the project's has at least the following VHDL files in directory vivado:

project.vhd	Original VHDL design with Xilinx I/O interface for data type and generics
project.do	ModelSim VHDL stimuli files for design with GSR delay
project_tb.vhd	The 7 section VHDL testbench file including data stimuli
project_tb.do	ModelSim stimuli files for testbench with GSR delay and no data stimuli
project tb msim.gif	The snapshot of the VHDL ModelSim TB simulation

Only for the FPU an ISIM timing simulation had been added since the XSIM simulation did not show the expected results. In total you will find over 250 files in the VHDL folder. The Verilog files in directory vvivado are:

project.v	Driginal Verilog design with Xilinx I/O parameter
project.do	IodelSim Verilog stimuli files for design with GSR delay
project_tb.v	The 5 section Verilog testbench file including data stimuli
project_tb.do	IodelSim stimuli file for testbench with GSR delay and no data stimuli
<pre>project_vtb_msim.gif</pre>	The snapshot of the Verilog ModelSim TB simulation
project_vtb_behav.gi	The snapshot of the Verilog behavior Vivado TB simulation
project_vtb_behav.wc	The waveform file of the Verilog behavior Vivado TB simulation
<pre>project_vtb_time.gif</pre>	The snapshot of the Verilog timing Vivado TB simulation
<pre>project_vtb_time.wcf</pre>	The waveform file of the Verilog timing Vivado TB simulation

In total you will find over 420 files in the Verilog folder. Only a few designs needed additional files such as memory initializations (e.g., fun\_text or fft256) and some need longer input testbench data such as dwtden, ica, or pca.

#### REFERENCES

[1] U. Meyer-Baese, "Digital Signal Processing with Field Programmable Gate Arrays", *Springer, Heidelberg* 2015.

[2] Visual Software Solutions, Inc. "HDL Bencher User's Guide" 60 pages.

[3] M. Hamid, "Writing Efficient Testbenches", Xilinx XAAP199, May 2010.

# Chapter 1:

#### 1.1 example



example_tb_time_impl.wcfg					_ 🗆 🖉 ×
<b>→</b>					370.000 ns
Rame	Value	0 ns .	100 ns .	200 ns .	300 ns .
Input data:					
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S (example_tb/reset	0				
📩 ⊡ 📲 /example_tb/a[7:0]	3		3		1 3
Kample_tb/b[7:0]	2	(		2	
▶ 표··· ▶ /example_tb/op1[7:0]	10	1	0	X o	
Output data:					
	12	·0	X	12X	<u>212</u>
<pre>example_ub/c[7:0]</pre>	5	·			
	50	<u> </u>	^°	<u> </u>	
	30			30	
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		(c)			
Fig. 1.1: Simulation for example.	mple. The	example code s	shows differe	ent HDL codin	ng styles such as data
flow (concurrent), sequential,	and compo	nent instantiation	s, see Fig. 1.	25 in 4/e. (a) V	VHDL ModelSim

simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

#### 1.2 fun\_text



17



Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

# Chapter 2

### 2.1 cmul7p8

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	) (	1	2	4	7	14	-1	-2	-4	-7	-14
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Fig. 2.1: Simulation for	<b>r</b> cmul 7p8	. The ev	aluatio	n is fro	m left t	o right	and the	e quanti	zation	error is	s larger
						~	~	- gound			

if the division (and rounding) is done first. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 2.2 add1p



**Fig. 2.2:** Simulation for add1p. The carry chain delay is improved if the adder is broken in two parts. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 2.3 add2p



2.4 add3p

#### 1073741820 351843720888 32760 10 X32770 X32760 X1073741820 X1073741830 X1073741820 X35184372088830 Х 32760 35184372088840 35184372088830 ÷ X Х Now 300 ns ursor 1 .00 ns (a)

#### **DSP** with FPGAs/4e

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ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

#### 2.5 div\_res



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**Fig. 2.5:** Simulation for div\_res. Division using the restoring principle, i.e., if a partial result is negative a correction is done to produce a positive restored value. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variable "r" is not available in the timing simulation.

#### 2.6 div\_aegp

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/div_aegp_tb/UUT/States/x	320	0	),384	307	<u>)</u> 320	
♦ /div_aegp_tb/UUT/States/t	255	0	307	245	255	
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🔍 🐻 /div aegp tb/dk	0			-				
Single for the set of the set	0							
🕓 🖬 📲 /div_aegp_tb/UUT/States/count[1:0]	2		0		1		2	
🖶 🖼 /div_aegp_tb/UUT/state[1:0]	0	0	X	1		X :	2 X 0	
I I								
▶ III ····· ▲ /div_aegp_tb/n_in[8:0]	384	(		38	4			
/div_aegp_tb/d_in[8:0]	307	[		30	7			
/div_aegp_tb/UU1/States/x[9:0]	320		X_	384	307	_~	320	
	255		Ň		245	_^i	255	
🖟 🖬 📲 /div aegp tb/g out[8:0]	320			0			X 320	
→ T[31:0]	100			10	0			5
							i	
XI								-
z (	• • •	•	III					Þ
		(b)						
div_aegp_tb_time_impl.wcfg							2	X
→D							500.000 n	15 🔺
💾 Name Valu	ie .			1				
				200 ns			400 ns	
Im /div_aegp_tb/cik								
							2	
<pre>/uv_aegp_tb/UUT/count[1:0] 2 /uv_aegp_tb/UUT/count[1:0] 0</pre>			0 X		1		2 2 2 0	
Image: All v_aegp_tb/UUT/count[1:0]     2       Image: All v_aegp_tb/UUT/count[1:0]     0       Image: All v_aegp_tb/UUT/state[1:0]     0		0	• • X		1	) ) ) )	2 2 ( 0	
Image: Aliv_aegp_w/reset     0       Image: Aliv_aegp_tb/UUT/count[1:0]     2       Image: Aliv_aegp_tb/UUT/state[1:0]     0       Image: Aliv_aegp_tb/UUT/state[1:0]     0       Image: Aliv_aegp_tb/n_in[8:0]     384		0	0 	1	1		2 2 2 2 0	
Image: Adv_aegp_tb/UUT/count[1:0]       2         Image: Adv_aegp_tb/UUT/count[1:0]       2         Image: Adv_aegp_tb/UUT/state[1:0]       0         Image: Adv_aegp_tb/UUT/state[1:0]       0         Image: Adv_aegp_tb/n_in[8:0]       384         Image: Adv_aegp_tb/d_in[8:0]       307		0	0 X	1 384 307	1		2	
Image: Aliv_aegp_tb/UUT/count[1:0]       2         Image: Aliv_aegp_tb/UUT/state[1:0]       0         Image: Aliv_aegp_tb/n_in[8:0]       384         Image: Aliv_aegp_tb/d_in[8:0]       307         Image: Aliv_aegp_tb/UUT/x[9:0]       384		0	• X	1 384 307	1		2 2 ) 0 384	
Image: Aliv_aegp_tb/UUT/count[1:0]       2         Image: Aliv_aegp_tb/UUT/count[1:0]       2         Image: Aliv_aegp_tb/UUT/state[1:0]       0         Image: Aliv_aegp_tb/n_in[8:0]       384         Image: Aliv_aegp_tb/d_in[8:0]       307         Image: Aliv_aegp_tb/UUT/x[9:0]       384		0 384 307	• X	1 384 307 307 X 245 X	1 320 255		2 2 0 384 307	
Image: Adiv_aegp_tb/UUT/count[1:0]       2         Image: Adiv_aegp_tb/UUT/count[1:0]       2         Image: Adiv_aegp_tb/UUT/state[1:0]       0         Image: Adiv_aegp_tb/n_in[8:0]       384         Image: Adiv_aegp_tb/d_in[8:0]       307         Image: Adiv_aegp_tb/d_in[8:0]       307         Image: Adiv_aegp_tb/d_in[8:0]       307         Image: Adiv_aegp_tb/UUT/x[9:0]       384         Image: Adiv_aegp_tb/UUT/x[9:0]       307         Image: Adiv_aegp_tb/UUT/t[9:0]       307         Image: Adiv_aegp_tb/UUT/t[9:0]       307         Image: Adiv_aegp_tb/UUT/t[9:0]       307         Image: Adiv_aegp_tb/UUT/t[9:0]       307		0 384 307		1 384 307 307 X 245 X	1 320 255		2 2 0 384 307	
Image: All v_aegp_tb/UUT/count[1:0]       2         Image: All v_aegp_tb/UUT/state[1:0]       0         Image: All v_aegp_tb/n_in[8:0]       384         Image: All v_aegp_tb/d_in[8:0]       307         Image: All v_aegp_tb/UUT/x[9:0]       384         Image: All v_aegp_tb/UUT/x[9:0]       384         Image: All v_aegp_tb/UUT/x[9:0]       307         Image: All v_aegp_tb/UUT/x[9:0]       307         Image: All v_aegp_tb/UUT/x[9:0]       307         Image: All v_aegp_tb/UUT/x[9:0]       307         Image: All v_aegp_tb/Q_out[8:0]       320         Image: All v_aegp_tb/Q_out[8:0]       320		0 384 307	• X	1 384 307 307 X 245 X	1 320 255		2 2 0 384 307 320	
iminiv_aegp_tb/UUT/count[1:0]       2         iminiv_aegp_tb/UUT/state[1:0]       0         iminiv_aegp_tb/n_in[8:0]       384         iminiv_aegp_tb/d_in[8:0]       307         iminiv_aegp_tb/UUT/x[9:0]       307         iminiv_aegp_tb/UUT/x[9:0]       384         iminiv_aegp_tb/UUT/x[9:0]       307         iminiv_aegp_tb/UUT/x[9:0]       307         iminiv_aegp_tb/UUT/t[9:0]       307         iminiv_aegp_tb/q_out[8:0]       320         iminiv_aegp_tb/T[31:0]       100		0 384 307		1 1 384 307 245 0 100	1 320 255		2 2 ) 0 384 307 320	
Image: All of a constraint of a		0 384 307	• X	307 X 245 X 100	1 320 255		2 2 ) 0 384 307 320	
Image: All of		0 384 307		1 1 384 307 245 0 100	1 320 255		2 2 )( 0 384 307 ( 320	

**Fig. 2.6:** Simulation for div\_aegp. Division using the method from Anderson, Earle, Goldschmidt, and Powers for 1.5/1.2 using a finite state machine with three processing steps sufficient for 8-bit precision. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The Verilog simulations (b/c) show integer values for the machine state while VHDL (a) uses literate coding.

### Xilinx HDL Manual

### 2.7 fpu

Trutts:       - </th <th>/fpu_tb/UUT/op fix</th> <th>2fp</th> <th>fix2fp</th> <th>ff</th> <th>2fix</th> <th>add</th> <th>sub</th> <th>mul</th> <th>div</th> <th>rec</th> <th>scale</th>	/fpu_tb/UUT/op fix	2fp	fix2fp	ff	2fix	add	sub	mul	div	rec	scale
Image: bytest     000000000000000000000000000000000000	· <b>⊥</b> - → /fpu_tb/sel 0		0	1		2	3	4	5	6	7
Image: Market State       Value       Value<	· <b></b> → /fpu_tb/dataa 00	010000	00010000	3	800000	<u> 3EAAAAAB</u>					
1       000000000000000000000000000000000000		XXXXXXX				3F2AAAAB					
Clubb         File         File <t< td=""><td>+</td><td>000000</td><td>00000000</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>00000001</td></t<>	+	000000	00000000								00000001
Now         900 mg         100 mg         200 mg         200 mg         900 mg <td></td> <td>800000</td> <td>3F800000</td> <td></td> <td>0010000</td> <td>3F800000</td> <td>BEAAAAAB</td> <td>3E638E3A</td> <td>3F000000</td> <td>40400000</td> <td>3F2AAAAB</td>		800000	3F800000		0010000	3F800000	BEAAAAAB	3E638E3A	3F000000	40400000	3F2AAAAB
100ms       200ms       200ms       200ms       200ms       200ms       000ms       000ms <td< td=""><td>Now</td><td>000 pc</td><td>milini</td><td></td><td>mhim</td><td>l Liriliii</td><td></td><td></td><td></td><td></td><td></td></td<>	Now	000 pc	milini		mhim	l Liriliii					
(a) fu_b_beav.wcfg	age Cursor 1	0.00 ns	) ns 100 0.00 ns	<u>0 ns 200 n</u>	is 300	<u>) ns 40</u>	0 ns 50	0 ns 60	0 ns 70	<u>0 ns 80</u>	<u>0 ns 900 ns</u>
fpu_b_behav.wcfg	·					(a)					
Image       Value       0       ns       1000 ns       600 ns       800 ns       800 ns       800 ns       800 ns       100 ns       1	fpu_tb_behav.wcfg										_ 🗆 🖉 🗙
Hame       Value       0 ns       200 ns       400 ns       600 ns       800 ns         10 ns       fsz2p       fsz2p       fsz2p       fsz2p       fsz2p       fsz2p         11 ns       fszzp       fszzp       fszzp       fszzp       fszzp       fszzp         11 ns       fszzp       fszzp       fszzp       fszzp       fszzp       fszzp         12 ns       fszzp       fszzp       fszzp       fszzp       fszzp       fszzp       fszzp         12 ns       fszzp	<b>→</b> D										1,000 ^
Image: constraint of the second of the se	Name Name	Value	0 ns		200 ns		400 ns	.	600 ns .	8	00 ns .
Imputs:       0       1       2       3       4       5       6       7       0         1       1       1       0       0       1       2       3       4       5       6       7       0         1 <td< td=""><td>🔍 🖓 op</td><td>fix2fp</td><td></td><td>fix2fp</td><td>fp2fix</td><td>bbe X</td><td>sub</td><td>X mul</td><td>div V</td><td>rec</td><td>scale X</td></td<>	🔍 🖓 op	fix2fp		fix2fp	fp2fix	bbe X	sub	X mul	div V	rec	scale X
Image: state of the	Inputs:								<u> </u>	/L	
Image: state of the state	🔍 🖪 📲 /fpu_tb/sel[3:0]	0		0	¥ 1	χ 2	Хз	$\langle 4 \rangle$	5)	6 X	7 X0
Image: state of the state	🙏 🗉 📲 /fpu_tb/dataa[31:0	] 000100	00 00	00010000	X 3£80000	οχ		3eaa	aaab		
Image: state of the state	<b>⊡</b> - 🔣 /fpu_tb/datab[31:0	] xxxxxxx	xx	xxxxxxxxx				3f2a	aaab		
Dutput:       37800000       318000000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       31800000       3180000000       318000000       318000000	▶ 🖽 📲 /fpu_tb/n[31:0]	000000	00			000	00000				0000001 (
ar //pu_tb/result[31:0]       3f800000	output:										
Image: The Theorem 100000 fs       100000 fs         Image: The Theorem 100000 fs       Image: Theorem 100000 fs         Image: The Theorem 100000 fs       Image: Theorem 100000 fs         Image: The Theorem 100000 fs       Image: Theorem 100000 fs         Image: The Theorem 100000 fs       Image: Theorem 100000 fs         Image: The Theorem 100000 fs       Image: Theorem 100000 fs         Image: Theorem 100000 fs       Image: Theorem 1000000 fs         Image: Theorem 100000 fs<	🚔 🖪 📲 /fpu_tb/result[31:0	] 3f8000	00 (	3£800000	0001000	0)(3£800000	) beaaaaab	(3e638e3a)	(3£000000)	40400000	3f2aaaab)(
Image: second	June 16 T	100000	) fs				100000 f	s			
Image: Input::     Image: Imput::     Imput:: <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></td<>											
(b) fu_tb_time_impl.wcfg											
(b)		F 4	• •						101010101010101010101010101	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
fpu_b_time_impl.wcfg      X         Yalue       0 ns       200 ns       400 ns       600 ns       800 ns         Inputs:       0       0       1       2       3       4       5       6       7         0       0       1       2       3       4       5       6       7         0       0       1       2       3       4       5       6       7         0       0       1       2       3       4       5       6       7         0       0       1       2       3       4       5       6       7         0       00010000       3f800000       3eaaaab       00000000       3eaaaab       00000000         00000000       00000000       00000000       3f800000       00000000       00000000         0       00000000       00000000       3f800000       00000000       3fe38e3a       000228a2a       000000000         100000 fs			Landard			(h)					
fpu_b_time_impl.wcfg    X       Name     Value       Inputs:        Inputs:        1						(0)					
Name       Value       0 ns       200 ns       400 ns       600 ns       800 ns         Inputs:       0 0       0       0       1       2       3       4       5       6       7         Imputs:       0       0       0       1       2       3       4       5       6       7         Imputs:       0       0       0       1       2       3       4       5       6       7         Imputs:       0       0       0       1       2       3       4       5       6       7         Imputs:       0       0       1       2       3       4       5       6       7         Imputs:       0       0       1       2       3       4       5       6       7         Imputs:       0       0       0       1       2       3       4       5       6       7         Imputs:       0 <t< td=""><td>fpu_tb_time_impl.wcfg</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>_ 🗆 🖓 ×</td></t<>	fpu_tb_time_impl.wcfg										_ 🗆 🖓 ×
Name       Value       0       ns       200 ns       400 ns       600 ns       800 ns         Inputs:       Inputs:       0       0       1       2       3       4       5       6       7         Inputs:       0       0       1       2       3       4       5       6       7         Inputs:       0       0       1       2       3       4       5       6       7         Inputs:       0       0       1       2       3       4       5       6       7         Inputs:       0       0       1       2       3       4       5       6       7         Inputs:       0       0       1       2       3       4       5       6       7         Inputs:       0       0       0       1       2       3       4       5       6       7         Inputs:       0       0       0       0       3       3       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0	→D									9	00.000 ns 🔺
Inputs:     0     1     2     3     4     5     6     7       1     //fpu_tb/sel[3:0]     0     0001000     3f800000     3eaaaaab     00000000       1     2     3     4     5     6     7       1     //fpu_tb/sel[3:0]     0     00010000     3f800000     3eaaaaab       1     1     2     3     4     5     6     7       1     1     00010000     3f800000     3eaaaaab     00000000       000000000     000000000     3f2aaaab     00000000     00000000       00000000     3f800000     00000000     3fe33e3a     00228a2a       1     1000000 fs     1000000 fs     1000000 fs     1000000 fs	Name	Va	lue		1200		400		1600		1990
Inputs:       0       0       1       2       3       4       5       6       7         Image: Mipu_tb/sel[3:0]       0       00       1       2       3       4       5       6       7         Image: Mipu_tb/dataa[31:0]       00010000       3f800000       3eaaaaab       3eaaaaab       3f2aaaab       000000001         Image: Mipu_tb/n[31:0]       00000000       000000000       402aaaab       00000000       3fe3Be3a       00228a2a       000000000         Image: Mipu_tb/result[31:0]       3f800000       3f800000       402aaaab       00000000       3fe3Be3a       00228a2a       000000000         Image: Mipu_tb/result[31:0]       3f800000       3fe800000       402aaaab       00000000       3fe3Be3a       00228a2a       000000000         Image: Mipu_tb/result[31:0]       3f800000       3fe800000       402aaaab       00000000       3fe3Be3a       00228a2a       000000000         Image: Mipu_tb/result[31:0]       3fe800000       Image: Mipu_tb/result[31:0]       3fe800000       Image: Mipu_tb/result[31:0]       Image: Mipu_tb/result[31:0]       Image: Mipu_tb/result[31:0]       Image: Mipu_tb/result[31:0]       Image: Mipu_tb/result[31:0]       Image: Mipu_tb/result[31:0]       Image: Mipu_tb/resultb/result[31:0]       Image: Mipu_tb/result[31:0]	Q+				- 200 MS		400 ms		600 ns	1	
Image: Arpu_Ebysel(3:0)       0       0       1       2       3       4       5       6       7         Image: Arpu_Ebysel(3:0)       00010000       00010000       3f800000       3eaaaaab       3eaaaaab         Image: Arpu_Eb/dataa[31:0]       00010000       00010000       3f800000       3f2aaaab       00000001         Image: Arpu_Eb/n[31:0]       00000000       00000000       00000000       00000000       000000000         Image: Arpu_Eb/n[31:0]       3f800000       3f800000       000000000       3fe38e3a       000228a2a       000000000         Image: Arpu_Eb/result[31:0]       3f800000       3f800000       402aaaab       00000000       3fe38e3a       000228a2a       000000000         Image: Arpu_Eb/result[31:0]       3f800000       3fe800000       402aaaab       00000000       3fe38e3a       000228a2a       000000000         Image: Arpu_Eb/result[31:0]       3f800000       3fe800000       3fe800000       3fe800000       3fe800000       3fe800000       3fe800000       000000000       3fe88e3a       000228a2a       000000000       4002aaaab       00000000       3fe88e3a       000228a2a       000000000       4002aaaab       00000000       3fe88e3a       000000000       4000000000       400000000       4000000000											
Image: Market 131:01     00010000     00010000     3f800000)     3eaaaaab       Image: Market 131:01     00000000     00010000     3f800000)     3f2aaaab       Image: Market 131:01     00000000     00000000     00000000       Image: Market 131:01     3f800000     3f800000     3fe38e3a       Image: Market 131:01     3f800000     3fe300000     3fe38e3a       Image: Market 131:01     3fe300000     3fe300000     3fe38e3a       Image: Market 131:01     3fe300000     3fe300000000     3fe38e3a       Image: Market 131:01     3fe300000     3fe38e3a     000228a2a       Image: Market 131:01     3fe30000     3fe38e3a     000228a2a       Image: Market 131:01     3fe38e3a     000228a2a     000000000       Image: Market 131:01     100000 fs     100000 fs     100000 fs	trpu_tb/sei[3:0]	0		0		X2		<u> </u>	<u> </u>	X	
X     i <td>E Market Catal 31:</td> <td>000 000</td> <td></td> <td>00010000</td> <td><u>3f8000</u></td> <td><u> </u></td> <td></td> <td>3es</td> <td>aaaab</td> <td></td> <td></td>	E Market Catal 31:	000 000		00010000	<u>3f8000</u>	<u> </u>		3es	aaaab		
<ul> <li></li></ul>	K ⊞ ··· · · · · · · · · · · · · · · · ·			×>>>>>>>>>	~	X		3f2	2aaaab		
Output:     3f800000     3f800000     3f800000     3f800000     3f800000     3fe38e3a     000228a2a     00000000       Image: State Sta	[ <b>q</b> ] <u>H</u> <b>*%</b> /tpu_tb/n[31:0]	0000	00000			0	0000000				00000001
1     3f800000     3f800000     X 00000000     X 402aaaab X 00000000     X 3fe3Be3a     X 000228a2a X 00000000       1     100000 fs     100000 fs     100000 fs     100000 fs     Image: Second	Output:										
	The pu_tb/result[31:	0] 3f80	0000	3f800000		000)(402aaa	ab <u>X</u> 0000000	10)(3fe	:38e3a	X00228a2a	0000000
	🚖 🤚 🛄	100	000 fs				100000	fs			
	4										
											-
		• •	• •		III						F.
						(c)					

#### **DSP** with FPGAs/4e

#### **Xilinx HDL Manual**

									900.000 ns
Name	Value	0 ns	200 ns		400 ns		600 ns		800 ns
sel[3:0] 😽 😽	0	0	<b>X</b> 1	X 2	X <u>3</u>	4	(5)	( <u>6</u> )	7
🔉 式 dataa[31:0]	00010000	000 10000	3f800000	X		3eaa	aaab		
🛌 😽 datab[31:0]	xxxxxxx	XXXXXXXXX				3f2a	aab		
<b>n</b> [31:0]	0000000			0000	0000				00000001
result[31:0]	3f2aaaab	3f800000	00010000	) X 3f8000	00 🚺 beaaaaab	3e638e3a	X 3f000000	40400000	3f2aaaab
15 t	100000 ps				100000 ps				
									<b>-</b> -
		X1: 900.000 ns							
<u> 2</u>	N A	• • III							

**Fig. 2.7:** Simulation of the design fpu. The design uses the ieee\_proposed library by David Bishop. Eight basic floating point operations are applied to the input values 1/3 and 2/3 as shown in the "op" row in the VHDL simulation. (a) VHDL ModelSim simulation. (b) Vivado VHDL behavior simulation. (c) Vivado VHDL timing simulation with errors. (d) ISIM VHDL timing simulation. Note that the Vivado timing simulation shows errors. Currently there is no equivalent library available for Verilog designs.

#### 2.8 cordic

🔶 /cordic_tb/clk	0								
/cordic_tb/reset	1								
	-41	-41							
➡-	55	55							
	0	0						(111	
🛨	0	0			14	<u>,40</u>	85	123	
Image: with the second sec	0	0						<u>(9</u>	
/cordic_tb/UUT/P1/x(0)	0	0		(55					
/cordic_tb/UUT/P1/y(0)	0	0		41					
/cordic_tb/UUT/P1/x(1)	0	0			<u>/96</u>				
/cordic_tb/UUT/P1/y(1)	0	0			<u>)</u> -14				
/cordic_tb/UUT/P1/x(2)	0	0				<u>(103</u>			
/cordic_tb/UUT/P1/y(2)	0	0				34			
/cordic_tb/UUT/P1/x(3)	0	0					<u>(111</u>		
/cordic_tb/UUT/P1/y(3)	0	0					)9		
<u> </u>									
A R ON	400 ns	) ns 50	ns 100	)ns 150	ins 200	ins 250	)ns 300	ns 350 n	s
🗟 🖉 🤤 Cursor 1	.00 ns	0.00 ns							
				(a)					



representation that yield radius (r=111) and phase (phi=123). The error is eps=9. This is a pipelined implementation and the rotation can be monitored in the behavior simulation. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The pipeline register "x" and "y" are not visible in the Vivado timing simulation (c).

#### 2.9 arctan



arctan_tb_time_impl.wcfg		_ ㅁ ァ ×
<b>→</b>		750.000 ns
Rame	Value	0 ns  500 ns
🔧 🖞 /arctan_tb/dk	1	
Iii /arctan_tb/reset	0	
🔧 🖽 📲 /arctan_tb/x_in[8:0]	255	-256 (-128 0 128 255
▲	1	1
■ 📲 /arctan_tb/d_o4[8:0]	1	
🖕 ऺ॒ 🔤 📲 /arctan_tb/d_o3[8:0]	-12	<u>-13</u> <u>-9</u> <u>-12</u> <u>-13</u> <u>-12</u> <u>-12</u>
	-24	
	177	<u> 225 ¥ 181 X 211 X 225 ¥ 211 ¥ 177</u>
III III (arctan_tb/f_out[8:0]	200	
t[31:0]	100	100
↓ >	<►	4
		(c)
2.2.9: Simulation for arc	tan. For	five values: $0, \pm 0.5, \pm 1$ the arctan function is computed using a

Chebyshev approximation. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 2.10 ln

✓ /In_tb/clk	0										ſ		
/In_tb/reset	1												
	0	0		16384	32768		49152		65536	5			
N													
_ <b>∓</b> –� /In_∞/f_out	0	0	1			14624		26572		36675	<u> </u>	45427	
A 🛤 🐑 🔹 Now	300 ns	ns	200	) ns		400	ns			600	ns		
🗟 🖉 🥥 Cursor 1	.00 ns	0.00 ns											
	1			(a)									-

ln_tb_behav.wcfg		_ D 2 ×
<b>20</b>		800.000
Name Name	Value	0 ns  200 ns  400 ns  600 ns
<sup>2⁺</sup> <sup>™</sup> /ln_tb/dk	0	
1/2 /n_tb/reset	0	
	65536	<u> </u>
I ■ I / In_tb/f_out[17:0]	45427	0 X 1 X 14624 X 26572 X 36675 X 45427
▶ <b>표</b> ····································	100	100
12		
±		
	4 F	4
C	· · · · · · · · · · · · · · · · · · ·	(b)
In_tb_time_impl.wcfg		_ ם אַ ×
<u>}</u>		800.000
Name	Value	0 ns  200 ns  400 ns  600 ns
1 /n_tb/dk	0	
	0 65536	0 16384 32768 49152 65536
٨		
Image: A transformed and the second seco	45427	
	100	
± ₽		
E 4 F	4 F	<
		(c)

**Fig. 2.10:** Simulation for ln. For five values: 0, 0.25, 0.5, 0.75, and 1.0 the natural logarithm function is computed using a Chebyshev approximation. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

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### 2.11 sqrt

♦ /sqrt_tb/dk	0												
↓ /sqrt_tb/reset	1												
🔷 /sqrt_tb/UUT/s	start	start	)leftsh	ift		sop					)rightshi	ift Idone	start
Isqrt_tb/UUT/op	load	load		scale	)nop	load	mac				denorm	n juop	
Image: sqrt_tb/count_o	0	0		(1	2	3							
🖅	3072	3072											
🖅	8	8											
🖅	24576	0				2457	6						
+	11585	11585											
+	4	0	(4				)3	2	(1	<u>)</u> 0	-1		
+	3072	0	3072	-3778	}		1581	3 -291	29 4229	7563			
+	11585	0		8			2457	6			11585		
+	0	0		3072	2457	6	-3778	3 (1298	0 (-1939	4 27754	28378	(1003	2
+	0	0											(10032
🛎 📰 💿 🛛 Now	300 ns	inn inn i	200	ins	400	) ns	600	ns	800	ns	1000+	ni i i i i i i i i i ns	1200 pc
🔓 🌽 🤤 🛛 Cursor 1	.00 ns	0.00 ps	200	-110	-100	7115	000	110		118	10001	15	1200 HS
		0100110				$(\mathbf{a})$							
						(a)							
sqrt_tb_behav.wcfg	anananananan	uararanananan ar	arararararara	ararararara	avaranavaranav		warararararara		awararararara		ararararara		_ 🗆 🖓 ×
<b>→</b>												1,	250.000 ns 🔺
Name		Value	0 ns	2	00 ns ,	400	ns	600 ns		800 ns ,	1,0	000 ns	1,20
Qt 1 lb /sqrt_tb/dk	1												
Q- 16 /sqrt_tb/reset	0												
🔍 🎞 📲 /sqrt_tb/UUT/s[3:0]	1				1		Х		2		_X	X 4	
sqrt_tb/UUT/op[3:0]	0			0	2	_X_4_	X		1		X	_X	4
<pre>Image: Image: Imag</pre>	0			Ó	X1	_X2	Х			3			
I sart tb/x in[16:0]	3	072						3072					
1 ■ Noprt_tb/pre_o[16:0]	8							8					
🚉 🖪 📲 /sqrt_tb/x_o[16:0]	2	4576			0		χ			24576			
📲 🖬 📲 /sqrt_tb/post_o[16:0]	1	1585						11585					
🖪 📲 /sqrt_tb/ind_o[3:0]	4		0			4	X		2 )	1 / 0		15	
grt_tb/imm_o[16:0]	3	072	<u> </u>	307:	<u> </u>	-3778	X	15813	-29129 ( 42	299 (		7563	
sqrt_tb/a_o[16:0]	1	1585		0	X	8	X		24576		X	11585	
					V 2072	V _2	1576 V	127294 V	12979 11	1677 V 222	2 V 28977	V	0032
[2] H d /sart tb/f o[16:0]	1	0032		n –		A 1 4	A	A	TES 12 VII			A 1	0002
<b>3</b> ■ ♥ /sqrt_tb/f_o[16:0] <b>a</b> ♥ /sqrt_tb/f_out[16:0]	10 10	0032 0032		0				0					X 10032
Image: Sqrt_tb/f_o[16:0]           Image: Sqrt_tb/f_out[16:0]           Image: Sqrt_tb/f_out[16:0]           Image: Sqrt_tb/f_out[16:0]	10 10 11	0032 0032 00						0 100					<u>) 10032</u>
<pre>/l = *** /sqrt_b/f_o[16:0]</pre>	1 1 1	0032 0032 00		0				0 100					<u>) 10032</u>
<pre>//L II ■ M /sqrt_B/f_0[16:0]</pre>	14 14 11	0032 0032 00						0 100					<u>) 10032</u>
(][ □ ♥ /sqrt_b/f_o[16:0] □ ♥ /sqrt_b/f_out[16:0] □ ♥ /[31:0]		0032 0032 00						0 100					<u>10032</u>
<pre>//L ■ ** /sqrt_b/f_0[16:0] ■ ** /sqrt_b/f_out[16:0] ■ ** T[31:0]</pre>	1) 1) 1	0032 0032 00	· · · · · · · · · · · · · · · · · · ·					0 100					<u>× 10032</u> 

sqrt_tb_time_impl.wcfg		א פ ם –
<b>→</b> D		1,250.000 ns
Rame	Value	0 ns   200 ns   400 ns   600 ns   800 ns   1,000 ns   1,2
🔍 🐌 /sqrt_tb/clk	1	
🔍 👍 /sqrt_tb/reset	0	
💢 🖬 📲 /sqrt_tb/UUT/s[2:0]	0	
▲ III - Nort_tb/count_o[1:0]	3	
🔄 🖬 📲 /sqrt_tb/x_in[16:0]	3072	3072
🛛 🖬 📲 /sqrt_tb/pre_o[16:0]	8	
🖆 🖬 📲 /sqrt_tb/x_o[16:0]	24576	0 24576
🖻 🖪 📲 /sqrt_tb/post_o[16:0]	11585	14585
Ⅲ /sqrt_tb/ind_o[3:0]	15	
📴 🖬 /sqrt_tb/imm_o[16:0]	7563	0 <u>30</u> 72 <u>-3778</u> <u>15813 -29129 42299 7563</u>
<pre>Image: Image: Imag</pre>	11585	
🛶 🖩 📲 /sqrt_tb/f_o[16:0]	10032	0
📶 🎞 📲 /sqrt_tb/f_out[16:0]	10032	0 χ100β2
	100	100
4 Þ	٠	
		(c)

**Fig. 2.11:** Simulation for sqrt. The input value x =0.75/8 =3072/32768 is first normalized and the square root is compute using a finite state machine with a final post processing operation. The Verilog simulation shows plain number instead of literal for the machine state. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local signal "op" cannot be found in the timing netlist.

#### 2.12 magnitude

/magnitude_tb/clk	0 1											
	1000	1000		707	0	-707	-1000	-707	0	707	0	
	0	0		707	1000	707	<u>jo</u>	-707	-1000	-707	0	
	0	0		<u>,1000</u>	883	<u>)</u> 1000	883	<u>)</u> 1000	883	<u>(1000</u>	883	)0
A 📰 🐑 Now	100 ns	) ns	200	ns	400	) ns	600	) ns	800	) ns	1000	) ns
🗟 ⁄ \ominus 🛛 Cursor 1	.00 ns	0.00 ns										
	·				(a)							

magnitude_tb_behav.wcfg		×
₽D		1,100.000 *
Name	Value	
Iiii /magnitude_tb/dk       Iiii /magnitude_tb/ck       Iiii /magnitude_tb/reset       Iiii /magnitude_tb/reset	0 0 0	
🖳 🎫 /magnitude_tb/y[15:0]	0	0 707 1000 707 0 -707 -1000 -707 0
🔰 🗉 📲 /magnitude_tb/r[15:0]	0	0 1000 8\$3 1000 8\$3 1000 8\$3 1000 8\$3 1000 8\$3
▶ <b>±</b> ··· <b>·</b> • <b>· T</b> [31:0]	100	100
12		
z (	< F	× ₩
		(b)
magnitude to time impl.wcfg		X
<b>₽</b>		1,100.000 ^
Name Name	Value	0 ns  200 ns  400 ns  600 ns  800 ns  1 00
<ul> <li>Im /magnitude_tb/dk</li> <li>Im /magnitude_tb/reset</li> </ul>	0 0	
S 🖪 🖓 /magnitude_tb/x[15:0]	0	
🕵 🖪 📲 /magnitude_tb/y[15:0]	0	0 <u>707</u> <u>1000</u> 707 <u>0</u> <u>-707</u> <u>-1000</u> <u>-707</u> <u>0</u>
magnitude_tb/r[15:0]	0	
	100	
12		
2		
z 4 F	4 F	
		(c)
<b>T</b> ! <b>A 1A</b> (C) <b>1</b> (C)		

 $\max(x,y)+\min(x,y)/4$  and tested for 9 angles at  $k*\pi/4$ . (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

# Chapter 3

### 3.1 fir\_gen

	0									
🔶 /fir_gen_tb/reset	1									
🔶 /fir_gen_tb/Load_x	0									
— Inputs: ———										
💶 - 🔶 /fir_gen_tb/x_in	0	0			(100	0				
💶 🔶 /fir_gen_tb/c_in	0	0	124 214	57 -33						
Local:										
🛨 /fir_gen_tb/UUT/x	0	0			(100	0				
=	{0} {0} {0} {0}	<u>{0} {0} {0} {0} </u>	X{0} X{0}	\{0} \{12	4} {214} {57} {	33}				
🛓 - 🔷 (0)	0	0		<u>(124</u>						
🛓 - 🔷 (1)	0	0		(124 )(214						
🛓 - 🔷 (2)	0	0	124	1 214 57						
🛓 - 🔷 (3)	0	0	124 214	1 <u>(</u> 57 )-33						
=	{0} {0} {0} {0}	<del>{0} {0} {0} {0} {</del> 0}			(12	){0} {0}	- {0} {0	}		
	0	0			(124	0 0				
<u>↓</u> -◆ (1)	0	0			214	0 0				
🛓 - 🔷 (2)	0	0			, <mark>57</mark> 0	0 0				
🛓 - 🔷 (3)	0	0			)-33(	0 0				
=	{0} {0} {0} {0}	<u>{0} {0} {0} {0} </u>				<u>{</u> 12	<u>{21</u>	<b>}{57 }{-3</b>	3 <u>){0} {0} {0</u> }	{0}
😐 - 🔷 (0)	0	0				12400	21400	5700 -33	00 )0	
😐 - 🔶 (1)	0	0				21400	5700	) <del>-3300</del> )0		
😐 - 🔶 (2)	0	0				5700	)-3300	)0		
😐-🔷 (3)	0	0				-3300	<u>)</u> 0			
Outputs:										
+	0	0				48	83	<u>)22 )-13</u>	<u>lo</u>	
Now	750 ns	) ns	200	) ns	400	ns	u da	600	) ns	l i i i
🗟 🎤 😑 🛛 Cursor 1	0.00 ns	0.00 ns								
			(	a)						

#### **DSP** with FPGAs/4e

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						750.000
Name	Value					
			200 ns		ns	600 ns
16 /fir_gen_tb/clk						
<pre>imagen_to/reset</pre>						
toad_x						
Inputs:						
$= \frac{1}{2} \sqrt{\frac{1}{2}}		0 124	V 214 V 57 V		-32	
Local:			<u></u>			
±-₩ x[8:0]			0	X 100 X	0	
	124,214,5	0,0,0,0 X 0,	0 X 0, 0 X 0, 1 X		124,214,57,-33	
<b>⊡</b> ¶[0][8:0]	124				124	
🖬 📲 [1][8:0]	214	0	) 124 )		214	
🖽 📲 [2][8:0]	57	0	X 124 X 214 X		57	
🖬 📲 [3][8:0]	-33	0 / 1	24 214 57		-33	
■ 📲 p[0:3][17:0]	0,0,0,0		0,0,0	(124)	0,0,	0,0
⊞ 🥰 [0][17:0]	•		0	(12400)	0	
<b>⊞</b> ·· <b>₩</b> [1][17:0]	•		0	(21400)	0	
🖽 📲 [2][17:0]	• C		0	5700	0	
🖽 📲 [3][17:0]	•		0	<u> </u>	0	
a[0:3][18:0]	0,0,0,0		0,0,0	X	<u>124 X 214 X 570 X -</u>	33 X 0,0,0,0
<b>⊞ </b> ₩ [0][18:0]	• ( <u></u>		0	X	12400 (21400 ( 5700 ) -:	3300 ( 0
			0	X	21400 × 5700 × -3300 ×	0
E™ [2][18:0]					<u>5700 X-3300 X</u>	0
Outputs:			•	^		0
			0	v	48 V 83 V 22 V	-13 \ 0
T[31:0]	50			50		
	کا <u>محمد ال</u>					
1	• • •					
			(b)			
gen_tb_time_impl.wcfg				uarananananananananana	ararateatararateatarateatarateata	2
						750.0
Name	Value	0 ns	200 ns	5 ,	400 ns	600 ns ,
🐻 /fir_gen_tb/dk	0					
1% /fir gen th/reset						
i /fir gen th/load	~ I					
i gen_b/coad	_^ _					
Inputs:						
	8:0] 0	(	0	χ 10	<u>•                                    </u>	0
🖬 📲 /fir_gen_tb/c_in[	8:0] -33	( <u> </u>	<u> 124 214 57</u>	(	-33	
<b>O</b> 1 1						
Outputs:	t[10:0] 0		0		48 83 2	2 Х-13 Х О
Outputs:				50		
Outputs: 	50					
outputs:	50					
Outputs: 	50					
Outputs: ■-™ /fir_gen_tb/y_ou ¤-₩ T[31:0]	50					
Outputs: 	50	▶ <				

**Fig. 3.1:** Simulation for fir\_gen. This is a generic FIR filter design that allows to load first different coefficients and then after Load\_x goes high performs filtering. In the example a length four filter is simulated with Daubechies length 4 wavelet filter coefficients. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variables "x, c, p"

#### and "a" are not available in the timing simulation.

#### 3.2 fir\_srg


fir_srg_tb_time_impl.wcfg		~ ×
<b>≥</b> 0		700.000 ns
Name Name	Value	0 ns   200 ns   400 ns   600 ns
State 15 / 16 / 16 / 16 / 16 / 16 / 16 / 16 /	0	
🎽 🚡 /fir_srg_tb/reset	0	
💫 🖬 📲 /fir_srg_tb/x[7:0]	0	
[	100	
	100	
	< •	→ 4
		(c)

**Fig. 3.2:** Simulation for fir\_srg. A length four filter with coefficients -1,3.75,3.75,-1 is used. This is a starting point design that can be further optimized by using coefficient symmetry, CSD coding, and pipelining. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variable "tap" is not available in the timing simulation.

#### 3.3 dasign





**Fig. 3.3:** Simulation for dasign. A signed distributed arithmetic sum-of-product computation is simulated for three coefficients  $\{-2,3,1\}$  three input word  $x=\{1,-3,7\}$  with each having 4 bits. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variables "x2[0], x1[0],x0[0]" and "p" are not available in the timing simulation.

# 3.4 dapara

🔶 /dapara_tb/clk	1						
/dapara_tb/reset	1						
+	0000	0000	0001	1101	0111	0000	
	000	000	<u> </u>	<u>(110</u>	<u></u>	)011	
+	000	000		Viaa	<u>)100</u>	2010	
$+$ /dapara_tb/UUT/x(2)	000	000		<u>,100</u>	110	,011	
	000	000		<u>,100</u> Υ1	7010	<u></u>	
		0		^±	<u>/v</u>	<u>^</u>	
🛎 📰 💿 🛛 Now	550 ns	i i i i i i i i i i i i i i i i i i i	200	) ns	40	l i i i i i i i i i i i i i i i i i i i	
🔂 🌽 😑 Cursor 1	.00 ns	0.00 ns	200	7110		5115	
			(a)				
dapara_tb_behav.wcfg			,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			₽	×
→D						550.000 ns	-
Rame Name	Value	10 mg		1200 mg		1400 mg	
	1						
With the set of the	0						
/dapara tb/x in[3:0]	0000	0000	V 0001	1101	V 0111	0000	
	001,001,001	,000,000,	000,000 × 100	,000, X 110,	000, \ 111,	100, X 011,010,	
Image: Image	001	00	• X	100 / 1	.10 / 1	11 ) 011	
▶	001		000			00 010	
💑 🖪 📲 /dapara_tb/UUT/x[2][2:0]	001		000	ı	.00 / 1	10 / 011	
🙀 🖬 🖏 /dapara_tb/UUT/x[3][2:0]	000		000		.00 ) 0	0 / 001	
📕 🖩 📲 /dapara_tb/y[6:0]	27		0		1	0 / -4	
T[31:0]	100			100			
							-
4 111 5	•				1. · · · · · · · · · · · · · · · · · · ·		-
			(b)				-
dapara_tb_time_impl.wcfg	raharaharaharahara			ahaahaahaahaahaahaa		~ ×	4
<b>→</b> □						550.000 ns 🔺	
Name	Value	10		1000	1.		
Q+		0 ns		200 ns	<u> </u>	100 ns	
🔰 🕼 /dapara_tb/clk	1						
🔪 🖓 /dapara_tb/reset	0						
🔼 🖪 🖏 /dapara_tb/x_in[3:0]	0000	0000	0001	1101	0111	0000	
🔍 🖪 📲 /dapara_tb/y[6:0]	-4		0		1 ) 0		
[ <b>√</b> ■	100			100			
70							
						-	
z ( )	•	+ -	III			•	

(c)

**Fig. 3.4:** Simulation for dapara. This is a parallel implementation of the distributed arithmetic sum-ofproduct computation. The design has three coefficients  $\{-2,3,1\}$  and three input word  $x=\{1,-3,7\}$  each having 4 bits. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variables "x[0],x[1],x[2]" and "x[3]" are not available in the timing simulation.

# Chapter 4

4.1 iir



Fig. 4.1: Simulation of the filter response to an impulse 1000 for iir is shown. This is a first order IIR filter with a pole at z=0.75. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. For Verilog a negative impulse was used to verify the correct sign extensions.

#### 4.2 iir\_pipe

<ul> <li>/iir_pipe_tb/dk</li> <li>/iir_pipe_tb/reset</li> </ul>	0 1											
➡-� /iir_pipe_tb/x_in	0	0	1000 )0									
- A Pr. 1. 11 / 1				·····	V				V== V	V==V==	V V	
+	<u> </u>	0		<u>1000 1750 1750 1750 1750 1750 1750 1750 </u>	) <u>1562 1</u> 42	1 1316 123	<u>6 1177 113</u>	<u>2 199 174</u>	<u>155 141</u>	<u>130 122</u>	<u>,16 ,12</u>	<u>,19 ,6</u>
🗠 🛒 💿 🛛 Now	1150 ns	ins in the second s	200	) ns	40	liiiiiiii Ons	60	) ns	800	) ns	100	liiiiiiiiii Ons
🗟 🌽 🤤 🛛 Cursor 1	0.00 ns	0.00 ns										
					(:	a)						

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iir_pipe_tb_behav.wcfg		בם – ×
<b>→</b> ]		1,151 ^
Name	Value	0 ns
<pre>     //ir_pipe_tb/clk     //ir_pipe_tb/reset </pre>	0	
II → II /ir_pipe_tb/x_in[14:0]     II → II /ir pipe tb/y out[14:0]     II → II /ir pipe tb/y out[14:0]	0	
► T[31:0]	50	
12		
	F 4	
		(b)
iir_pipe_tb_time_impl.wcfg		× ۾ ם _
₹D		1. *
Name	Value	0 ns  200 ns  400 ns  600 ns  800 ns  1,000
16 /iir_pipe_tb/dk	0	
Nir_pipe_to/reset		
💃 🖬 🖏 /iir_pipe_tb/x_in[14:0]	0	
Image: Second state         Image: Second state	4 50	
12		
	• 4	
		(c)
<b>Eta 4.2</b> Cincelation	. f	
<b>Fig. 4.2:</b> Simulation	llor llr_	_pipe. This is a look-anead pipelined lossy integrator with an effective pole
at $z=0.75$ . The respo	onse to an	impulse 1000 of the IIR first order filter is shown. (a) VHDL ModelSim
simulation. (b) Viva	ido Verilo	g behavior simulation. (c) Vivado Verilog timing simulation.

## 4.3 iir\_par

<ul> <li>√iir_par_tb/clk</li> <li>√iir_par_tb/reset</li> <li>√iir_par_tb/clk2</li> </ul>	0 1 0											
<pre>       /iir_par_tb/UUT/state       //iir_par_tb/x in       //iir_par_tb/x in       //iir_par_tb/x in       //iir_par_tb/x</pre>	even 0	even 0	<u>)od</u> o 1100	d <u>Jeven</u> ) 10	<u>)odd jever</u>	) jodd	)even )odd	)even jo	dd <u>leven lodd</u>	<u>keven</u> kodd	)even jodd	jeven jodd
	0	0 0	<u>(100</u>	)0 	<u>)o</u>							
uir_par_tb/y_e ₽-৵ /iir_par_tb/y_o	0 0	0 0					<u>,750</u> ,1000	<u>)</u> 421 )562	236 )316	<u>)</u> 132 )177	)74 )99	)41 )55
	0	0						<u>(1000 )</u> 7	50 <u>(</u> 562 (421	<u>)316 )236</u>	<u> 177 132 (132</u>	<u>)99 )</u> 74 )
Now Now	630 ns	) ns	100 ns	lu	200 ns		300	ns	400 ns		500 ns	600 ns
🔒 🌽 🤤 Cursor 1	0.00 ns	0.00 ns				\ \						
					(	a)						

## **Xilinx HDL Manual**



**Fig. 4.3:** Simulation for iir\_par. This is a parallel implementation of the IIR filter with a pole at *z*=0.75. The response to an impulse 1000 of the first order IIR filter is shown. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variable "state" is not available in the timing simulation.

## 4.4 iir5sfix

## **Xilinx HDL Manual**



iir5sfix_tb_behav.wcfg		_ D 2 ×
<b>&gt;</b> ]		0.150000 us
Name	Value	0 us 20 us 40 us 60 us
Im fir5sfix_tb/reset       Im fir5sfix_tb/switch       Imput Data:	0 1	
Analog y_out:	-325597	
<b>≟</b>	19	
<sup>→</sup>	100	
×	<b>∢</b> . ►	<►
		(b)
iir5sfix_tb_time_impl.wcfg		×
<b>→</b> D		0.150000 us
Name       Image: state sta	Value 1 0 1	0 us  20 us  40 us  60 us   1   1   1   1   1   1   1   1   1
	0000000040000000 0	
	0	

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(c)

**Fig. 4.4:** Simulation of the impulse response for iir5sfix. This is a 5. order direct form IIR filter design that was implemented using the sfixed type in VHDL and without special data type in Verilog. (a) VHDL ModelSim impulse response. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

## 4.5 iir5para





iir5para_tb_time_impl.wcfg		×
¥D		65.000000 us
Name	Value	0 us .  20 us .  40 us .  60 us
🔍 🐚 /iir5para_tb/clk	0	
🔍 🔏 /iir5para_tb/reset	0	
🔍 🛯 🖓 /iir5para_tb/switch	1	
Input Data:		
United American (1997)	65536	65536
E M / Jir5para tb/y Dout[31:0]	19	19
12		
<u>수</u>		
🔐 🖪 📲 /iir5para_tb/y_1out[31:0]	70381	
E.		
- <b>F</b>		
🛄 🖬 📲 /iir5para_tb/y_21out[31:0]	-731	
🖪 📲 /iir5para_tb/y_22out[31:0]	-4512	
⊡ 📲 /iir5para_tb/y_out[31:0]	65225	
<b>T</b> [21,0]	100	
m	100	
4	4	
	· ·	

**Fig. 4.5:** Simulation of a step response for iir5para. This is a 5. order parallel implementation of a narrow band IIR filter design that was implemented using the sfixed type in VHDL and without special data type in Verilog. (a) VHDL ModelSim step response. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

## 4.6 iir5lwdf





VHDL and without special data type in Verilog. (a) VHDL ModelSim step response. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

# <u>Chapter 5</u>

# 5.1 db4poly

<ul> <li>/db4poly_tb/dk</li> <li>/db4poly_tb/reset</li> <li>/db4poly_tb/ck2</li> <li>/db4poly_tb/UUT/state</li> </ul> Idb4poly_tb/X_in Idb4poly_tb/x_e Idb4poly_tb/x_e Idb4poly_tb/x_o	0 1 o even 0 0 0	even 0 0 0	)odd )ev )1	en )odd 2)3 )2 )1	)even)@ )even)@ 	odd )ev	<u>en )odd</u>	(100)	 ddev 		) (even) 0 (0	odd )ev	en )odd j		odd <u>l</u> ev	en jor
·	0	0			248	61	0	228	<u>(12</u>	400	<b>(5700</b>	<u>)</u> 0				
·	0	0			214	(60	9	)-99	)0			21	400	-3300	<u>)</u> 0	
/db4poly_tb/y_out	0	0				<u>(1</u>		(4	) <mark>0</mark>		(48	22		83	)-1	2
≗≣⊛ Now	100 ns				mim	400		mlm	 600		ulu				100	
⊖ ∠ursor 1	.00 ns	0.00 ns	200	7 TIS		400	TIS		600	TIS		800	TIS		100	ons
					(	(a)										
db4poly_tb_behav.wcfg         Image: State of the st	Value			0 ns 1				00) () () () () () () () () () (	600 ns 0 10 12400	5 100) 100) 5700 0 148		800 ns	0		000 ns 000 ns 000 ns 000 ns 000 ns	
					(	(b)										

db4poly_tb_time_impl.wcfg		
		1,100.000 ns
🕄 Name	Value	0 ns .  200 ns .  400 ns .  600 ns .  800 ns .  1.000 ns
4 /db4poly_tb/clk	0	
4 /db4poly_tb/reset	0	
🔍 🛛 🖟 /db4poly_tb/dk2	0	
Å.		
◀ ⊞10 /db4poly_tb/x_in[7:0]	0	
▶ 표-₩ /db4poly_tb/x_e[16:0]	0	
👷 🖽 📲 /db4poly_tb/x_o[16:0]	0	
🚖 º ™ /db4poly_tb/g0[16:0]	0	0 248 (610 228 12400 5700 ) 0
	0	<u> </u>
db4poly_tb/y_out[8:0]	0	
	50	
SIL		· · · · · · · · · · · · · · · · · · ·
•	<b>∢</b> ►	
		(c)

**Fig. 5.1:** Simulation for db4poly. A polyphase decomposition is demonstrated for the length 4 Daubechies filter. The triangular input shows the splitting in even and odd inputs and the impulse of 100 at even and odd index inputs shows the "not time invariant" behavior of the system. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variable "state" is not available in the Vivado simulation, but clk2 can be used as representation for the state variable.

## 5.2 cic3r32

♦ /cic3r32_tb/dk	0												
🔶 /cic3r32_tb/reset	0	1											
🔶 /cic3r32_tb/dk2	0		<u>)                                    </u>					1			1		
🔶 /cic3r32_tb/UUT/count	13												
₽_	127	127											
	50292												
III //i1 //i1 III //i	993												
	294												
	-28	0	570865	5043297	17578705	24770239	16375729	10960417	30254225 (11	309825 )25	397617 95	70273 (-320	10671 )
	970	0		570865	5043297	17007840	-29813536 )	-1202976 -	31378208 (13	878496 )34	9408 (-48	56608 -173	9552 )9
	-20	0			570865	5043297	16436975	32252031 -	18210816 -1	564672 (15	81472 31	727616 -187	35104 )
_ <b></b> ◆ /cic3r32_tb/y_out	508	0				8 )	76 )	242 /4	15 (49	5 <u>(50</u>	7 <u>)</u> 50	3	
Now	200 pc				humm	huuuu	huuuu	1		humm			in
Now	JUUTIS	ns	200	0 ns	400	0 ns	600	00 ns	800	0 ns	100	00 ns	12000 ns
Cursor 1	.00 ns	0.00 ns											
						(a)							

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3r32_tb_behav.wcfg		_ 0
		12.
Name	Value	
		0 us 2 us 4 us 6 us 8 us 10 us
™ /cic3r32_tb/dk	0	
1 /cic3r32_tb/reset	0	
₩ /cic3r32_tb/dk2	0	
	13	
	127	127
	50292	
<pre>Image: Image: Imag</pre>	9932670	
	29422244	
	-28074815	<u> </u>
	-2088960	0 <u>X 570865 X</u> 5043297 X <u>16436</u> X <u>32252</u> X <u>-1821</u> X <u>-1564</u> X <u>15081</u> X <u>31727</u> X -
■ ····································	33292288	<u>μ</u> <u>χ</u> <u>570865 χ</u> 5043297 χ <u>15866</u> χ <u>27208</u> χ <u>32461</u> χ <u>33292</u> χ <u>33292</u> χ
₩ //:-0-00 /h//:/[0-0]		
	508	<u> </u>
₩	30	
1	, I.	
		(b)
r32_tb_time_impl.wcfg		
		12
Name	Value	
14 /cic3r32 tb/dk	0	
W /cic3r32 tb/reset	ő	
₩ /cic3r32_tb/dk2	0	
🖪 📲 /cic3r32_tb/UUT/count[4:0]	13	
🖪 📲 /cic3r32_tb/x_in[7:0]	127	127
■ /dic2:20 th / UT to[35.6]	50000	
dc3r32_b/001/l0_reg[25:0]	9932670	
	3332070	
/cic3r32_tb/UUT/i2_reg[25:0]	29422244	
■	29422244 -28074815	0 X 570865 (5043297 X17578705) -24770 X16375729 X10960417 X30254225 X1309825 X25397617 X 9570273 X -3
Image: Amage: Amage	29422244 -28074815 9700576	0 <u>570865</u> <u>5043297</u> <u>17578705</u> <u>-24770</u> <u>16375729</u> <u>10960417</u> <u>30254225</u> <u>11309825</u> <u>25397617</u> <u>9570273</u> <u>-3</u> 0 <u>570865</u> <u>5043297</u> <u>17007840</u> <u>-29813</u> <u>1202976</u> <u>-31378</u> <u>13878496</u> <u>349408</u> <u>-4856608</u> <u>-1</u>
Image: Mark and American Control (Control (Contro) (Contro) (Control (Contro) (Control (Control (Contro) (Contro) (	29422244 -28074815 9700576 -2088960	0         570865         5043297         17578705         -24770         (16375729         (10960417         (30254225         (1309825         (25397617         9570273         -3           0         570865         5043297         17007840         -29813         1202976         -31378         (18878496)         349408         -4856608         -1           0         570865         5043297         17007840         -29813         1202976         -31378         (18878496)         349408         -4856608         -1           0         570865         5043297         (16436975)         32252031         -18210         -1564672         (15081472)         3127616         -1
A (ac3r32 b/UT//2_reg[25:0]     A (ac3r32 b/UT//2_reg[25:0]     A (ac3r32 b/UT/c0[25:0]     A (ac3r32 b/UT/c1[25:0]     A (ac3r32 b/UT/c1[25:0]     A (ac3r32 b/UT/c2[25:0]     A (ac3r32 b/UT/c2	29422244 -28074815 9700576 -2088960	0         570865         5043297         \17578705         -24770         \16375729         \10960417         \30254225         \11309825         \25397617         9570273         -           0         \$70865         \$5043297         \17007840         -29813         \1202976         -31378         \18878496         349408         -4856608         -1           0         \$70865         \$5043297         \17007840         -29813         \1202976         -31378         \18878496         349408         -4856608         -1           0         \$70865         \$5043297         \16436975         \32252031         -18210         -1564672         \15081472         \3127616         -1
M /ac3r32_b/UT//2_reg[25:0]     M /ac3r32_b/UT//2[25:0]     M /ac3r32_b/UT/c0[25:0]     M /ac3r32_b/UT/c1[25:0]     M /ac3r32_b/UT/c2[25:0]     M /ac3r32_b/UT/c2[9:0]     M /ac3r32_b/_out[9:0]     M /ac3r32_b/UT/c2[9:0]	29422244 -28074815 9700576 -2088960 508	0         570865         5043297         \17578705         -24770         \16375729         \10960417         \30254225         \1309825         \25397617         9570273            0         \$70865         \$5043297         \17007840         -29813         \1202976         -31378         \13878496         349408         \-4856608         -1           0         \$70865         \$5043297         \17007840         -29813         \1202976         -31378         \13878496         349408         \-4856608         -1           0         \$70865         \$5043297         \16436975         \$32252031         -18210         \-564672         \15081472         \3127616         -1           0         \$70865         \$6043297         \16436975         \$32252031         -18210         \-564672         \15081472         \3127616         -1           0         \$70865         \$6043297         \16436975         \$2252031         -18210         \-564672         \15081472         \3127616         \-1           0         8         76         \$242         415         \$495         \$507         \$508           0         20
III       M /ac3r32_b/UUT//2_reg[25:0]         III       M /ac3r32_b/UUT/c0[25:0]         III       M /ac3r32_b/UUT/c1[25:0]         III       M /ac3r32_b/UUT/c2[25:0]	29422244 -28074815 9700576 -2088960 508 30	0         570865         5043297         \17578705         -24770         \16375729         \10960417         \300254225         \1309825         \25397617         9570273         -<
A / / / / / / / / / / / / / / / / /	29422244 -28074815 9700576 -2088960 508 30	0         570865         5043297         17578705         -24770         16375729         10960417         300254225         11309825         25397617         9270273         -           0         570865         5043297         17007840         -29813         1202976         -31378         13878496         349408         -4856608         -1           0          570865         5043297         17007840         -29813         1202976         -31378         13878496         349408         -4856608         -1           0          570865         5043297         16436975         32252031         -18210         -1564672         15081472         312727616         -1           0          570865         5043297         16436975         32252031         -18210         -1564672         15081472         312727616         -1           0          8         76         242         415         495         507         508           30          30           -         -         -         -         -         -         -         -         508         -         -         -         -         -
a         // /ci:3*32_b/UUT//2_reg[25:0]           a         // /ci:3*32_b/UUT/c0[25:0]           a         // /ci:3*32_b/UUT/c1[25:0]           a         // /ci:3*32_b/UUT/c2[25:0]	29422244 -28074815 9700576 -2088960 508 30 30 30	0       \$570865       \$5043297       (17578705)       -24770       )(16375729)       (10960417)       3009825       (25397617)       9970273       -         0       \$570865       \$5043297       (17007840)       -29813       +1202976       -31378       (13878496)       349408       >-4856608       -1         0       \$570865       \$5043297       (1636975)       \$2252031       -138210       -1564672       >15081472       >31727816       -1         0       \$570865       \$5043297       (16436975)       \$2252031       -18210       -1564672       >15081472       >31727816       -1         0       \$570865       \$5043297       (16436975)       \$2252031       -18210       -1564672       >507       \$508         0       \$8       76       242       415       495       \$507       \$508         30       30       30       30       30       30       30       30

**Fig. 5.2:** Simulation for cic3r32. A three stage CIC filter with full bit width in all stages is designed and tested with a step response as input. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. It is interesting to notice that all local signals are available too in timing simulation since this are register signals.

## 5.3 cic3s32

- 🚸	/cic3s32_tb/clk	0																								
- 🚸	/cic3s32_tb/reset	0																								
- 🔶	/cic3s32_tb/dk2	0																		1		1		1		
<b></b>	/cic3s32_tb/x_in	127	127																							
	/cic3s32_tb/y_out	508	0		)8))	76)	241	415	(495	508								) <mark>50</mark>	7	)508	}			507		)508
	New	100		1.1	1	1	1 1	1				1 1	1 1	1.1	1					 			1 1		1 1	
	NOW	JUUINS	) ns		500	0 ns				10	000 I	ns				1500	0 ns				2000	00 ns				25000 ns
🖻 🎤 😑	Cursor 1	.00 ns	0.00 ns																							
										(;	1)															

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cic3s32_tb_behav.wcfg			adaretie editera					sieredes sieredes										vianient		ן א ק ו	
₹D																		2	5.0000	<u> 10 us</u>	^
Name Name	Value	10 us			l5 us				10 us			11	.5 us			li	20 us				
A /cic3s32_tb/dk	o						· · ·														
Cic3s32_tb/reset	0	1																			
💫 🖟 /cic3s32_tb/dk2	0															1					
	127									1	27									<u></u>	
N ₩ M /dc3s32_b/y_out[9:0]	30		0	<u>X_8</u>	<u></u>	<u>241</u> X	415×49	<u>5 X</u>	<b> </b>	3	08	=	X	507	_X		08	X_	507	<u>×508</u>	
		<u></u>																			
																					-
÷ • •	- F	•				III															F
								(b)													
cic3s32_tb_time_impl.wcfg																		ananan	_ C	רק ב x	
€																				25	^
Rame	Va	lue	0 us				5 us			10	us			15	us			2	0 us		
Cic3s32_tb/dk	o				_	·	'		<u> </u>				<u> </u>			-	· · · ·				
/cic3s32_tb/reset	0																			_	
Wa /cic3s32_tb/ck2	0										197							Ц			
idess52_b/x_in[7:0]	508			0	)	8	76 (2	41 (415)	(495)		127	508			_χ	507	-χ-	50	)8		
Image: Provide the state of	30										30										
12																					
																					-
								(-)													
								(C)													
Fig. 5.3: Simulation	on for	cic3	s32	. A tł	nree	stag	ge C	IC fi	lter v	with	bit pi	run	ing i	n th	e L	SBs	is d	esig	gned	and	l
tested with a step r	respons	se as i	nput	. Not	tice t	he	quar	ntizat	ion i	n th	e out	out	togg	ling	g bet	twe	en 5	07 :	and $\sharp$	508.	
(a) VHDL Model	Sim s	imula	tion.	(b) V	/iva	do '	Veri	log b	ehav	ior	simul	atic	on. (	c) V	ivac	lo V	/eril	og	timiı	ng	

simulation.

## 5.4 rc\_sinc



sinc_tb_behav.wcfg			- 0 2
			9.000000 us
Name	Value	0 us  2 us  4 us  6 us	8 us
₩ /rc_sinc_tb/dk	0		
1/2 /rc_sinc_tb/reset	0		
	5	C0000000000000000000000000000000000000	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
10 /			
<pre>\mathcal{k} /rc_sinc_tb/ena_in_o</pre>	0		┙╘╡┡╬╘┙╘┙╚
We /rc_sinc_tb/ena_io_o			
	0		
🖪 📲 /rc_sinc_tb/f0_o[8:0]	0		χ
⊞\$ /rc_sinc_tb/f1_o[8:0]	0	0 20 60 20	X
	0		X -2 X0
	-2		<u> </u>
H=20 1[21:0]	100		
٠ .	۰ ۲	< III	
inc_tb_time_impl.wcfg			₽
			9.000000 us
Name	Value	0 us  2 us  4 us  6 us	8 us
₩ /rc_sinc_tb/dk	0		มากกกกุกกกกุกกกกุ
₩ /rc_sinc_tb/reset	0		
H. Marc_sinc_tb/count_o[3:0]	5		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
₩ /rc sinc tb/ena in o	0		
//rc_sinc_tb/ena_out_o	1		
¼a /rc_sinc_tb/ena_io_o	0		
	0	0 (10 (20 (30 (40 ) 50 (60 (70 (80 ) 70 (60 ) 50 (40 ) (30 ) (20 ) 10 ) 0	
			V
In the sine the life of the second			
	0		
<b>四 ─戦</b> /rc_sinc_tb/f0_o[8:0] <b>四 ─戦</b> /rc_sinc_tb/f1_o[8:0] <b>四 ─戦</b> /rc_sinc_tb/f2_o <u>[8:0]</u>	0 0 0	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	χ <u>ο</u> χ2χο
<ul> <li>□ - M /rc_sinc_tb/f0_o[8:0]</li> <li>□ - M /rc_sinc_tb/f1_o[8:0]</li> <li>□ - M /rc_sinc_tb/f2_o[8:0]</li> <li>□ - M /rc_sinc_tb/y_out[8:0]</li> </ul>	0 0 0 -2	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	X 0 X -2 X0 X 31 X 20 X 7 X -2
Image: Market M Market Market Mark	0 0 -2 100	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	X 0 X −2 X0 X 31 X 20 X 7 X −2
<sup>™</sup> /rc_sinc_b/f0_o(8:0] <sup>™</sup> /rc_sinc_b/f1_o(8:0] <sup>™</sup> /rc_sinc_b/f2_o(8:0] <sup>™</sup> /rc_sinc_b/f2_o(8:0] <sup>™</sup> /rc_sinc_b/y_out[8:0] <sup>™</sup> /[Si:0]	0 0 -2 100	0         X         20         60         X         20           0         X         20         60         X         20           0         X         7         46         73         X         31           0         X         -2         7         X         20         X         31           0         X         -2         X         7         X         20         X         31           0         X         -2         X         7         X         20         X         31           0         X         -2         X         7         X         20         X         X         46         X         73         X         60         X         46         X         10         X         40         46         X         X         X         X         40 <td>X 0 X -2 X0 X 31 X 20 X 7 X -2</td>	X 0 X -2 X0 X 31 X 20 X 7 X -2
■     M/rc_sinc_b/f0_o(8:0]       ■     M/rc_sinc_b/f1_o(8:0]       ■     M/rc_sinc_b/f2_o(8:0]       ■     M/rc_sinc_b/f2_o(8:0]       ■     M/rc_sinc_b/f2_o(8:0]       ■     M/rc_sinc_b/f2_o(8:0)	0 0 -2 100	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	X 0 X -2 X0 X 31 X 20 X 7 X -2

**Fig. 5.4:** Simulation for rc\_sinc. A *R*=3/4 rate change is implemented using three sinc FIR filters and tested with a triangular input signal. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

## 5.5 farrow

# DSP with FPGAs/4e

<pre>/farrow_tb/clk /farrow_tb/second</pre>	0	ហហ	mm	www	MM	huu	ww	ww	nuu	ww	ww	ww	ww	nun	ww	ww	ww	NNN
	0		XXXXX	xxxx				<u>r r r r</u>	<u>yyy</u> y	<u>yyyy</u>	<u>yyyy</u>	נניני				,,,,	<u>, , , , ,</u>	<u>y y y y</u>
<pre>/farrow_tb/ena_in_o</pre>	FALSE	ſ	يىر		പ്പ	ᅸᇿ	പ്പ	புட		νų	ഥ	ĽĽ	ייאב	டா		ЛЪ	്ന	ᆀᅳ
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📑 🖬 📲 /farrow_tb/c2_o[8:0]	0	<u> </u>
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		(c)
Fig. 5.5: Simulation fo	<b>r</b> farr	row. A R=3/4 rate change using Lagrange polynomials and a Farrow
combiner is tested with	a trian	gular input signal. (a) VHDL ModelSim simulation. (b) Vivado Verilog

behavior simulation. (c) Vivado Verilog timing simulation.

## 5.6 cmoms

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		(b)
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IIIII [+3 T[31:0]	100	100
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**Fig. 5.6:** Simulation for cmoms. The cubic C-MOMS splines principle for smooth interpolation is shown for a triangular input signal. Note that a IIR compensations filter is required by the C-MOMS. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

## 5.7 db4latti

## Xilinx HDL Manual



**Fig. 5.7:** Simulation for db4latti. A length 4 Daubechies lattice filter bank is designed and tested with impulses of 100 at even and odd inputs. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior

## simulation. (c) Vivado Verilog timing simulation.

#### 5.8 dwtden



#### **DSP** with FPGAs/4e





**Fig. 5.8:** Simulation for dwtden. This is a three level DWT denoising with three levels of thresholds. The signal structure is well preserved at high threshold values, i.e., few remaining wavelet coefficients. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

# Chapter 6

## 6.1 rader7



ader7_tb_time_impl.wcfg		<b>הם –</b>
		1,850.000 ns
Name	Value	0 ns  500 ns  1,000 ns  1,500 ns
k /rader7_tb/clk	1	
🚡 🕼 /rader7_tb/reset	0	
Inputs:		
🔪 🖽 📲 /rader7_tb/x_in[7:0]	0	
Local:		
🖪 📲 /rader7_tb/UUT/state[1:0]	1	
■ ■ 📲 /rader7_tb/UUT/count[4:0]	2	
🖪 📲 /rader7_tb/UUT/accu[10:0]	0	0 10 70 120 220 260 280 0
Outputs:		
🖽 📲 /rader7_tb/y_real[10:0]	0	0 X-35 X-36 X-35 X-36 X-35 X280 X 0
■ 📲 /rader7_tb/y_imag[10:0]	0	0 73 10 26 74 -11 -27 0
<b>⊞</b> ∎a <mark>T[31:0]</mark>	100	100
l		
K	- F	•
		(c)

**Fig. 6.1.1:** Simulation for rader7. The 7 point Rader DFT design is tested with a triangular input data. Due to the algorithm the values appear in permutated order at the input and a second time for the cyclic computation of the algorithm. The first valid out data appear after 1.1 µs. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

## 6.2 fft256



56_tb_behav.wcfg															
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Name	Value	10 us		10 us		20 us		30 us		40 us		150 1	15		60 us
₩ /fft256_tb/dk	1														
1 /fft256_tb/reset	0	1													
🗉 📲 /fft256_tb/UUT/States/count[8:0]	1							257							
፹··₩ /fft256_tb/UUT/s[2:0]	4	1													4
🖬 📲 /fft256_tb/stage_o[8:0]	9		1		2	3	4		5	6	$\sim$	7 X	8		9
∎ 📲 /fft256_tb/gcount_o[8:0]	0	0							000000		3 0			0	
Inputs:															
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🖬 📲 /fft256_tb/xi_in[15:0]	0							0							
Local:															
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🛛 📲 /fft256_tb/xr_out1[15:0]	-80					40					60	X 400 X		-30	
🖪 📲 /fft256_tb/xi_out1[15:0]	0							0							
🖬 📲 /fft256_tb/xr_out255[15:0]	695	X				0			X	92	_X	30 📈	-386		695
	73	( x				0			X	127	_X2	32	-44		73
± ₩ /fft256_tb/w_o[8:0]	0	( <u> </u>						000	XXXXXX	Y	X 0	X 64 X		0	
■ ₩ /fft256_tb/dw_o[8:0]	-256	<u> </u>	1	X_	2	4	<u>X                                     </u>	X	16 )	32	_X6	54 X	128		-256
u ₩ /fft256_tb/i1_o[8:0]	0	<u> </u>													0
■ ₩ /fft256_tb/i2_o[8:0]	1	128													1
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simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

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💶 - 🔶 /fft 256_tb/stage_o	0	0	1		
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	0	0			
Local:		-			
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🖬 📲 /fft256_tb/xi_out0[15:0]	0	X		0	
	40	X	X	40	
	0	X	X	0	
21 III - 12 /fft256_tb/xr_out255[15:0]	х		×		
	х		X		
	0	X	X	0	
■ ¶ /fft256_tb/dw_o[8:0]	1		1		
±	0		0		
	128		128		
■ M /fft256_tb/k2_c[8:0]	-250		-256		
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■ ¶ /fft256_tb/fftr[15:0]	0		0		
■	0		0		
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					P
			(b)		



**Fig. 6.2.2:** Simulation for fft256. The input data are 8 none zero values 20,40,60,... 160 followed by 248 zeros. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

<pre>/fft256_tb/dk     /fft256_tb/reset</pre>	1										
<pre>//ft256_tb/UUT/States/</pre>	count 1	ΪO	1	12	Ĭ3	4	Ĭ5	Ĭ6	¥7	18	Ĭ9
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+	1	1									
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/fft256_tb/fft_valid	1										
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🖬 📲 /fft256_tb/xr_out0[15:0]	720			720				
□ 1 /fft256_tb/xi_out0[15:0]	0			0				
🖪 📲 /fft256_tb/xr_out1[15:0]	-80			-80				
🗄 🎞 📲 /fft256_tb/xi_out1[15:0]	o			0				
📙 🖭 📲 /fft256_tb/xr_out255[15:0]	695	χ		695				
🖪 🖭 📲 /fft256_tb/xi_out255[15:0]	73	λ <u> </u>		73				
፹₩ /fft256_tb/w_o[8:0]	o			0				
	-256	128		-256				
፹₩ /fft256_tb/i1_o[8:0]	o	254		0				
	1	255		1				
፹₩ /fft256_tb/k1_o[8:0]	2			2				
፹₩ /fft256_tb/k2_o[8:0]	1			1				
Outputs:								
■ 🦋 /fft256_tb/wo[8:0]	4			4				
냲 /fft256_tb/fft_valid	1							
■	0	0		8 64 192 32 1	.60 96 224 16			
⊑₩ /fft256_tb/fftr[15:0]	720	0	720 7.	0 ( 694 ( 661 ) 629 ( 5	76 ( 522 ( 455 ) 400			
	0	0	X	7 / -158 / -232 / -309 / -	371 ( -431 ( -478 ( -527			
H-4 T[31:0]	25			25				
•	* * *	•						

Name         Value           Name         Value           1         1           1/ft256_tb/stage_0[8:0]         1           1         1/ft256_tb/stage_0[8:0]         9           1         1/ft256_tb/stage_0[8:0]         9           1         1/ft256_tb/stage_0[8:0]         0           1         1         0           1         1         0           1         1         0           1         1         0           1         1         0           1         1         0           1         1	_time_impl.wcfg							. P
Jame         Value         S7,780 ns         S7,600			57,762.500	ns				
iii /ft256_tb/ck       1         iii /ft256_tb/rest       0         iii /ft256_tb/rest       1         iiii /ft256_tb/rest       1      <	me V	/alue 57	,750 ns	57,800 ns	57,850 ns	57,900 ns	57,950 ns	58,
1// fft256_b/reset       0         1// fft256_b/reset       1	/fft256_tb/dk 1							
1       1       1       2       3	/fft256_tb/reset 0							
1       1       0       0       0         1       1       0       0       0       0         1       1       0       0       0       0       0         1       1       1       0       0       0       0       0         1       1       1       0       0       0       0       0       0         1       1       1       1       0 <td< td=""><td>/fft256_tb/stage_o[8:0] 9</td><td>8</td><td></td><td></td><td>9</td><td></td><td></td><td></td></td<>	/fft256_tb/stage_o[8:0] 9	8			9			
Inputs:       0       0       0         Imputs:       0       0       0       0         Imputs:       0       0       0       0       0         Imputs:       0       0       0       0       0       0         Imputs:       0       0       0       0       0       0       0         Imputs:       0       0       0       0       0       0       0       0         Imputs:       0	/fft256_tb/gcount_o[8:0] 0				0			
1       0       0         1       0       0       0         1       0       0       0       0       0 <t< td=""><td>iputs:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>	iputs:							
1       1       1       0       0         1       1       1       1       1       1         1       1       1       1       1       1       1         1       1       1       1       1       1       1       1         1	/fft256_tb/xr_in[15:0] 0				0			
Local:       720       720         1       /fft256_b/x_out0[15:0]       0       0         1       /fft256_b/x_out1[15:0]       -80       -80         1       /fft256_b/x_out1[15:0]       0       0         1       /fft256_b/x_out255[15:0]       695       695         1       /fft256_b/x_out255[15:0]       73       73         1       /fft256_b/x_out255[15:0]       73       0         1       /fft256_b/x_out255[15:0]       73       0         1       /fft256_b/x_out255[15:0]       73       0         1       /fft256_b/x_out255[15:0]       73       0         1       /fft256_b/x_ol8:0]       0       0         1       /fft256_b/x_ol8:0]       0	/fft256_tb/xi_in[15:0] 0				0			
1       /#t256_b/x_out0[15:0]       720         1       /#ft256_b/x_out0[15:0]       0         1       /#ft256_b/x_out1[15:0]       0         1       /#ft256_b/x_out255[15:0]       695         1       /#ft256_b/x_out255[15:0]       73         1       /#ft256_b/x_o[8:0]       0         1       /#ft256_b/x_o[8:0]       0         1       /#ft256_b/x_o[8:0]       0         1       /#ft256_b/x_o[8:0]       1         1       /#ft256_b/x_o[8:0]       1         1       //ft256_b/x_o[8:0]       0         1       //ft256_b/x_o[8:0]	ocal:							
Image: Arrow of the second	/fft256_tb/xr_out0[15:0] 720	0			720			
	/fft256_tb/xi_out0[15:0] 0				0			
Image: Microsoft (13:0)       0         Image: Microsoft (13:0)       695         Image: Microsoft (13:0)       695         Image: Microsoft (13:0)       695         Image: Microsoft (13:0)       73         Image: Microsoft (13:0)       0         Image: Microsoft (13:0)       1         Image: Microsoft (13:0)       0         Image: Microsoft (13:0)       0 <tdimage: (13:0)<="" microsoft="" td="">       0</tdimage:>	/fft256_tb/xr_out1[15:0] -80	° ∣			-80			
Image: Milling and the second seco	/mt256_m/xi_out1[15:0] ()				0			
Image: Application of the second s	/fft256_tb/vi_out255[15:0] 69:				695			
Image: Application of the second s	/fft256_tb/w_o[8:0] 0				/3			
Image: Application of the second s	/fft256 tb/dw o[8:0] 256	6 <b>-</b>			256			
Image: Application of the second s	/fft256 tb/i1 o[8:0] 0				0			
Image: Market	/fft256_tb/i2_o[8:0] 1	<u> </u>			1			
III · //fft256_tb/k2_0[8:0]       1         Outputs:       III · //ft256_tb/w0[8:0]       4         III · //ft256_tb/fft_valid       0         III · //ft256_tb/fft_valid       0         III · //ft256_tb/fft1[5:0]       0         III · //ft256_tb/fft1[15:0]       0         III · //ft256_tb/fft1[	/fft256_tb/k1_o[8:0] 2				2			
Outputs:       4         # /fft256_tb/wo[8:0]       4         # /fft256_tb/fft_valid       0         # /fft256_tb/rcount_o[8:0]       0         # /fft256_tb/fft[15:0]       0         0       128       64       192       32       160       96       23         0       720       710       694       661       629       \$76       522       48         0       720       710       694       661       629       \$76       522       48         0       720       710       694       661       629       \$76       522       48         0       720       710       694       661       629       \$76       522       48         0       777       7158       7309       731       7431       74         0       25       25       25       25       25       25       25	/fft256_tb/k2_o[8:0] 1				1			
Image: Market	utputs:							
1/2       //ft256_tb/ftf_valid       0       0       1/2       64       192       32       160       96       22         1/2       //ft256_tb/ftb/ft256_tb/ftb/ft550_       0       0       1/2       64       192       32       160       96       22         1/2       //ft256_tb/ftb/ft550_       0       0       1/2       64       192       32       160       96       22         1/2       //ft256_tb/ftb/ft550_       0       0       1/2       720       210       694       661       629       \$76       522       45         1/2       1/2       1/2       1/2       -1/2       -1/2       -3/2       1/2       41       -	/fft256_tb/wo[8:0] 4	1 X			4			
Image: Margin	/fft256_tb/fft_valid 0							
0       0	/fft256_tb/rcount_o[8:0] 0			28 64	192 ( 32 )	160 / 96 /	224 16 1	44
Im     M     /fft256_tb/fft0[15:0]     0     X     -77     X     -158     X     -232     X     -309     X     -431     X     -4       Im     M     T[31:0]     25     25     25     25     25	/fft256_tb/fftr[15:0] 0	0	<u> 720 (</u>	10 🗙 694 🐰	661 🗙 629 🗶	\$76 X 522 X	455 🗙 400 🗙 3	26
	/fft256_tb/ffti[15:0] 0		o <u>X</u> -	77 🗙 -158 🗶 -	-232 X -309 X ·	371 🗙 -431 🗶	-478 🗙 -527 🔪 -	556
	T[31:0] 25				25			
	• •	• <						
			(	(c)				

The DC part with  $\sum(x_i)=720$  is verified. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.
# Chapter 7

### 7.1 lfsr



behavior simulation. (c) Vivado Verilog timing simulation.

### 7.2 lfsr6s3

♦ /Ifsr6s ♦ /Ifsr6s ■ ♦ /Ifsr6s	3_tb/dk 3_tb/reset 3_tb/y	1 0 0		 )7	62	)55	) <u>60</u>	)39	)58	22	) (48	) )5	 )46	) (49	13	) (45	) (41	 _)8	) <u>4</u>	38	)50	) )21	) (40		了 7(
21 <b>23 (</b>	Now	400 ns	) ns	1.1	1	11	- 1 500	ns i	I I	1	1	.000	) ns	1.1	L I	1	i I 500	ns I	1.1	1	2	i I 000	ns i		1.1
🔒 🧨 😑	150 ns																					215	0 ns		
	(a)																								

lfsr6s3_tb_behav.wcfg		×
Image: Second system       Name         Image: Second system       Image: Second system         Image: Second system	Value 1 0 1 1 0 1 0 100	2,150.000 ns 0 ns 500 ns 1,000 ns 1,500 ns 2,000 ns 2,000 ns 0 7 -2 -9 -4 -25 -6 22 -16 \$ -18 -15 13 -19 -23 8 4 -26 -14 21 -24 0 7 - 100
4 >	<b>۲</b>	< <u>.</u> Ⅲ →
		(b)
lfsr6s3_tb_time_impl.wcfg		~
→ Name	-	
Image: state of the state o	Value 1 0 -24 100	0 ns 500 ns 1,000 ns 1,500 ns 2,000 hs 0 7 -2 -9 -4 -25 -6 22 -16 5 -18 -15 13 -19 -23 8 4 -26 -14 21 -24 0 7 100
Image: state of the state o	Value 1 0 -24 100	0 ns 500 ns 1,000 ns 1,500 ns 2,000 hs 0 0 7 -2 -9 -4 -25 -6 22 -16 5 -18 -15 /13 -19 -23 8 4 -26 -14 (21 -24 0 7) 100
Image: State of the state o	Value 1 0 -24 100 <	0 ns 500 ns 1,000 ns 1,500 ns 2,000 hs 0 7 -2 -9 -4 -25 -6 22 -16 5 -18 -15 (13 -19 -23 (8 4 -26 -14 21 -24 0 7) 100 100 (C)
Image: Affsr6s3_tb/clk         Image: Affsr6s3_tb/reset         Image: Affs	Value 1 0 -24 100 4 • • on for	0 ns 500 ns 1,000 ns 1,500 ns 2,000 hs 0 7 -2 -9 -4 -25 -6 22 -16 3 -18 -15 (13 -19 -23 (8) 4 -26 -14 (21 -24 (0) 7) 100 (c) 1fsr6s3. In the multistep (i.e., 3 in this case) linear feedback shift register

simulation the cycle length is reduced by a factor 3 to  $(2^{\circ}-1)/3=21$ . (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 7.3 ammod

/ammod_tb/dk /ammod_tb/reset	0 1																	
→ /ammod_b/r in	100	100									2	5						
+ /ammod tb/phi in	0	0			),30	160 <u>1</u> 90	1120 J150	J-180 J-1	50 <b>(-120</b> )-	-90 1-60	1-30 10	). 130	160 190	1120 X	150 1-18	30 - 150	-120 -9	0 1-60 1
	0	0	)-14 )-1	2 (-5			<u>ا</u>	3 )3	(5)-3	<u>)</u> 3 )-	5 )-3	)3 )-5	5 <u>)-3</u> )	3)-5	)-3	3 5	(-3	)3 )-5
+	0	0		(16	2		),	138 )87	(13 )-87	(-138)-	162 -138	3)-87 )1	3 )87 )	138 (40	34	22 4	-22	)-34 )-40
	0	0		(13	1		)a	37 (138	(162 )138	3)87)-	13 .87	)-138 )-1	162)-138)	-87 )4	22	34 40	34	)22 )-4
A R A	)00 ns							1.1.1				1 1 1						1 1 1 1
Set Ourson 1	00 ns	0.00 ps		500 ns		100	0 ns		1500	ns		200	00 ns		2	500 ns		
	100 113	0.00 115					$\langle \rangle$											
							(a)											
ammod_tb_behav.wcfg																	- 0	א קינ ב
<u>→</u>																	3,100.0	00 ns ^
Name Val	ue  0 n	s		500 ns		1,000 r	s		1,500 ns		2	,000 ns		2,	500 ns		_,	3,000
/ammod_tb/dk 0																		
(ammod_b/reset 0					100					Y				25				
🚴 ፹ 📲 /ammod_tb/phi_in[8:0] 0			0	х	30 ( 60 )	90 120 1	50 \-180 \-	150 - 120	-90 / -60	<u>(-30)</u>	30	60 ( 90	120 150	X-180 -1	.50 -120	<u>-90</u>	50 (-30)	
												·						
M mmod_mod_b/eps[8:0] 3 mmod_b/x out[8:0] -22		X	<u>14 X -12 X</u>		-5		X <u>-3 X 3</u> V 138 X 87	<u> </u>	X3X 7_V-138V-1	-5 <u>× -3 ×</u>	<u>3 X -5</u>	X -3 X : X 88 X 1:	3 X -5 X	-3 X 3 34 V 22	X_5_X X_4_X-:	-3 (3) 22 (-34)	(-5)(- (-41)(-3	
		0		Ê	13		87 136	162 13	7 88 -	12 -88	-137 -162	2)-138)-1	87 4	22 34		34 22	-2 -2	2
T[31:0]									100									
F-																		
I ( ) (	+ -				m													
							(h)											
							(0)											

ammod_tb_time_impl.wo	cfg																						_	02	×
<b>→</b>																							3,100	.000 ns	^
Name		Value	10 nc		1500 ne			11 000 w	-			1 500 m	e		12	000 %	-			12 50	0 ກະ			13 00	
State of the s	dk	0						1,000 1				.,								2,00				0,00	
Ammod_tb/r	reset	0	F																						
S 🖪 📲 /ammod_tb/r	_in[8:0]	25				10	0							X					25						
🙏 🖬 📲 /ammod_tb/p	ohi_in[8:0]	0		0		30 60	90	120 1	50 -180	)(-150)(	-120	-90 -	60 -30		30	60 ( 9	90 (12)	0 150	)(-180	-150	(-120)	-90 (-	60 -30	0 0	
I4											_											_			
▶ 🖽 📲 /ammod_tb/e	eps[8:0]	3	<u> </u>	<u> </u>		-5			<u>X -3 X</u>	3 / 5	_X-	3 🛛 3	X <u>-5 X</u>	<u>-3 X 3</u>	X -5	Х -з	<u>X_3</u> X	-5 X	-3 X	<u>‡ X</u>	<u>5</u> X -	<u>3 X 3</u>	X <u>-5</u> X	-3 (3	
🔁 🖽 📲 /ammod_tb/x	x_out[8:0]	-22	(	0	_X	162			X 138 X	87 X 13	3 X -≸	17 X-138	X-163 X-	-137 🗙 -8	8 X 12	X 88	X 137 X	40 X	34 X	22 X	4 X-2	2 🛛 -34	X -41 X	-35 X	
💁 🖽 📲 /ammod_tb/y	y_out[8:0]	-35	K	0	X	13			X 87 X :	138 🗶 16	2 🛛 1	17 🕺 88	X -12 X	-88 X-13	37X-162	2×-138	X -87 X	4 X	22 X	34 X	40 🛛 3	4 🛛 22	X -2 X	-22 X	
д 🖽 🖽 T[31:0]		100	(									100													
14m																									-
: (	۱.	< +	•																						•
									(c)	)															
										,															

**Fig. 7.3:** Simulation for ammod. The amplitude modulation has been implemented with the CORDIC algorithm. The simulation shows two amplitude values 100 and 25 and a linear increase by 30 degree phase (phi) which gives a cycle length of 12 clock cycles. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

## Chapter 8

### 8.1 fir\_lms



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**Fig. 8.1:** Simulation for fir\_lms. This is a two tap adaptive filter design that "learns" the coefficients  $f_0 = 43.3$  and  $f_1 = 25$ . (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 8.2 fir4dlms

<ul> <li>/fir4dlms_tb/dk</li> <li>/fir4dlms_tb/reset</li> </ul>	0 0	
— Input Data: Input Data: Input Data:	-111	64 111 1 64 1111 1 64 1111 1 64 1-111 1 64 1111 1 64 1-111 1 64 1111 1 64 1-111 1 64 1-111 1 64 1111 1 64 1111 1 64 1111 1 64
+	9	10 /60 /9 /-41 /10 /60 /10 /-39 /11 /60 /10 /-40 /10 /59 /9 /-41 /10 /60 /10 /-39 /11 /60 /10 /-40 /10 /59 /9
Locals:		
	43	
+	23	
Outputs:	_	
Image: Fire of the second	-2	0
Image: Provide the state of	12	
Þ		
Now Now	700 ns	Dins 500 ns 1000 ns 1500 ns 2000 ns 2500 ns
🗟 🌽 🤤 Cursor 1	700 ns	2700 ns
		(a)
fir4dlms_tb_behav.wcfg		고 교 고 2 200 000 - 2 - 2 - 2 - 2 - 2 - 2 - 2 -
fir4dlms_tb_behav.wcfg	Value	_ □ 코 × 2,700.000 ns 10 co co 10 co co co 10 co co co 10 co co co co co co co co co co co co co
fr4dlms_tb_behav.wcfg Э∏ Name Q t 1 // fr4dlms_tb/clk	Value 0	→ × 2,700.000 ns 0 ns 1,000 ns 1,000 ns 1,500 ns 2,500 ns 2,500 ns 2,500 ns 1,000
fir4dims_tb_behav.wcfg	Value 0 0 -111	C 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
fr4dims_tb_behav.wcfg           1           Name           1 <t< th=""><td>Value 0 -111 9</td><td>□ ns       1,000 ns       1,500 ns       2,000 ns       2,500 ns         0 ns       1,500 ns       2,000 ns       2,500 ns       2,500 ns         64 (111) -64 (-111) 64 (111) -64 (</td></t<>	Value 0 -111 9	□ ns       1,000 ns       1,500 ns       2,000 ns       2,500 ns         0 ns       1,500 ns       2,000 ns       2,500 ns       2,500 ns         64 (111) -64 (-111) 64 (111) -64 (
fir4dims_tb_behav.wcfg           Image: style="text-align: center;">Name           Image: style="text-align: center;">Image: style="text-align: center;"/>Image: style="text-align: center;"///Image: style="text-align: center;	Value 0 -111 9	L 11 -64 -111 64 111 -64 -111 64 -111 -64 -111 64 -111 -64 -111 64 -111 -64 -111 64 -111 -64 -111 64 -111 -6
fir4dims_tb_behav.wcfg       Image: State of the state of	Value 0 -111 9 43	
fir4dims_tb_behav.wcfg         >]]         Name         □       /fir4dims_tb/dk         □       /fir4dims_tb/ck         □       /fir4dims_tb/f0_out[7:0]	Value 0 -111 9 -43	- □ 7 × 2,700.000 ns 1,000 ns 1,500 ns 2,500 ns 2,
fir4dims_tb_behav.wcfg           Э]           Name           Iii           Iii           Iii           Iii           Iiii           Iiii           Iiiii           Iiiii           Iiiiii           Iiiiiii           Iiiiiiiiiii           Iiiiiiiiiiiii           Iiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii	Value 0 -111 9 43	
fr-ddms_tb_behav.wcfg           Image: state of the state of	Value 0 -111 9 43	
fir4dims_tb_behav.wcfg         Image: Second Secon	Value 0 -111 9 43 23	
fr4dims_tb_behav.wcfg         Image: style st	2 Value 0 0 -111 9 43 23	
fir4dims_tb_behav.wcfg         ?]         Name         ?:	Value 0 -111 9 -113 9 -2	L 50 ns 1,000 ns 1,000 ns 1,000 ns 1,000 ns 2,000 n
fir4dims_tb_behav.wcfg         ?]         Name	Value 0 -111 9 43 23 -2	
fir4dims_tb_behav.wcfg         Pir         Name         Image: The set in the	Value 0 -1111 9 -3 -2 -2	$\begin{array}{c c c c c c c c c c c c c c c c c c c $
fir4dims_tb_behav.wcfg         Image: state of the s	Value 0 0 -111 9 43 23 -2 12 100	0       ns       1,000 ns       1,000 ns       1,000 ns       2,500 ns       2,500 ns       2,500 ns         64       111       64       10       55       9       41       10       60       10       10       10       10       10       10       10       10       10       10       10       10
fir4dims_tb_behav.wcfg         Image: State of the state of the	Value 0 0 -111 9 43 23 -2 12 100	L 200 ns 2,700.000 ns 4,500 ns 2,500 ns 2,
fir4dims_tb_behav.wcfg         ???         Name         ????????         ????????????????????????????????????	Value           0           -111           9           43           23           -2           12           100	L 200 NS 2,700 ND NS 1,000 NS 1,000 NS 1,000 NS 1,000 NS 2,000 NS 2,0

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**Fig. 8.2:** Simulation for fir4dlms. This is a two tap pipelined delay adaptive filter design that "learns" the coefficients  $f_0$ = 43.3and  $f_1$ =25 at a higher clock speed due to additional pipeline registers with the cost of little more residual error. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 8.3 g711alaw

🔶 /g711alaw_tb/dk	0											1
🧇 /g711alaw_tb/reset	1		1									
Input:												
Image: Participation of the second secon	0	0	64	128	256	512	1024	4095	4160	4224	4352	2
/g711alaw_tb/sign	0											
· → /g711alaw_tb/x	0	0	64	128	256	512	1024	4095	64	128	256	4
— Local: —	_											
	0	0	32	48	64	180	196	127	[160	176	192	4
·	1	1	66	132	264	528	1056	4032	4162	4228	4360	4
/g711alaw_tb/dec_sign	0											
	1	1	66	132	264	528	1056	4032	66	132	264	
Error:												
💶 🤣 /g711alaw_tb/err	1	1	2	4	8	16	32	63	2	4	8	2
≌	000 ns	) ns	20	iliiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii	، ا ا ا ا ا ا 40	i li i i i i i i i 10 ns	60	dininini Oins		iliiiiiii )0 ns	1000 100	luu )0 ns
🔂 🖉 😑 Cursor 1	.00 ns	0.00 ns										
				(	a)							

711alaw_tb_behav.wcfg											_ D @ >
<u>*0</u>										1,00	00.000 ns
Name	Value	0 ns	1	200 ns	1	400 ns	1	600 ns	1	800 ns	
/ /g711alaw_tb/dk	0										
Input:	0										
👖 🖽 /g711alaw_tb/x_in[12	:0] 4352	0	X 64	128	256	512	1024	4095	4160	4224	X 4352
The sign	1										
	256	(	X64	<u> </u>	X256	<u> 512</u>	X_1024	<u> 4095</u>	χ 64	<u> 128</u>	X_256_
⊆ <u>∎</u> № /g711alaw_tb/enc[7:0	)] 192	0	) 32	48	64	80	X 96	127	X 160	176	X 192
🛂 🖽 📲 /g711alaw_tb/dec[12:	:0] 4360		66	132	264	528	1056	4032	4162	4228	4360
🖌 📜 dec_sign	1		V		V		V-1000				V
Error:	264		<u> </u>	<u>132</u>	<u> </u>	<u>k 528</u>	<u>X_1056</u>	<u>4032</u>	<u>X 66</u>	132	X264
📕 🖽 /g711alaw_tb/err[13:	0] 8	1	) <u> </u>	4	X <u>8</u>	16	X <u>32</u>	63	χ 2	4	X
H	100					1	00				
21											
4	+ + 1										
· ·				(	h)						
				、	0,						
711alaw_tb_time_impl.wcfg					,						2
711alaw_tb_time_impl.wcfg					,					1,	_ [] 귀
711alaw_tb_time_impl.wcfg	Value 0	ns	20	0 ns	40	00 ns		600 ns	1	1,	_ [ 귀
711alaw_tb_time_impl.wcfg	Value o	ns	20	0 ns		00 ns	· · · · · · · ·	600 ns		1, 800 ns	_ [] 2 000.000 ns
711alaw_tb_time_impl.wcfg Name Name Name Name Name Name Name Name	Value 0 0	ns	20	0 ns	40	00 ns		600 ns		1, 800 ns	7
711alaw_tb_time_mpl.wcfg Name % /g711alaw_tb/clk % /g711alaw_tb/reset Input: # # /g711alaw_tb/x_in[12:0]	Value 0 0 0 4352	ns	64	0 ns	256	512 (	1024	600 ns 4095	4160	1,	_ ] 7 000.000 ns
711alaw_tb_time_impl.wcfg Name Name Name Name Name Name Name Name	Value 0 0 0 4352 1 256	ns	64 64	0 ns	256	512 X	1024	600 ns 4095	4160	1, 800 ns 4224 128	7 000.000 ns 1 ) 4352 ) 256
<pre>711alaw_tb_time_impl.wcfg 711alaw_tb_time_impl.wcfg % Name % Name % 1% /g711alaw_tb/clk % 1% /g711alaw_tb/reset % Input: % agn %</pre>	Value 0 0 0 4352 1 256	ns	64	0 ns 128 ( 128 )	256	512 X	1024	600 ns 4095 4095	4160	1, 800 ns 4224 128	_ ] 7 000.000 ns 
<pre>711alaw_tb_time_impl.wcfg  Name  Name  Name  Name  Name Name Name</pre>	Value 0 0 0 4352 1 256 192 4360	ns	64 64 32 66	0 ns 128 ( 128 ( 128 ( 128 ( 132 (	256 256 64	512 ( 512 ( 80 ( 528 (	1024 1024 96	600 ns 4095 4095 127 4032	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	1, 800 ns 4224 128 176 4228	_ □ 7 000.000 ns ↓ ↓ ↓ ↓ ↓ 4352 ↓ 256 ↓ 192 ¥ 4360
<pre>711alaw_tb_time_impl.wcfg      Name      Nam      Name      Name      Name      N</pre>	Value 0 0 0 4352 1 1 256 0 192 4360 1 1	ns 0 ( 0 ( 1 )	64 64 32 66	0 ns 128 ( 128 ( 128 ( 128 ( 128 ( 132 ( 132 ()	256 256 64 264	00 ns 512 X 512 X 512 X 80 X 528 X	1024 1024 96 1056	4095 4095 4095 4095 4095	(4160) (64) (64) (160) (4162)	1, 800 ns 4224 128 128 176 4228	_ □ 7 000.000 ns ↓ ↓ ↓ ↓ ↓ 4352 ↓ 256 ↓ 192 ↓ 4360
711alaw_tb_time_impl.wcfg Name Na	Value     0       0     0       0     0       4352     0       1     0       256     0       192     4360       1     0       264     0	ns 0 X 0 X 1 X	64 ( 64 ( 32 ( 66 (	0 ns 128 \ 128 \ 128 \ 128 \ 132 \times	256 256 64 264	00 ns	1024 1024 96 1056	600 ns 4095 4095 (127 (4032) (4032)	<pre>4160 4160 64 4160 4160 4160 4160 4162 66</pre>	1, 800 ns 4224 128 176 4228 132	_ □ 7       000.000 ns       1 + 1 + 1
711alaw_tb_time_impl.wcfg Name	Value 0 0 1 256 1 192 4360 1 264 8		64 ( 64 ( 64 ( 32 ( 66 ( 66 (	0 ns 128 ( 128 ( 128 ( 128 ( 128 ( 132	256 256 64 264 8	00 ns 512 X 512 X 512 X 528 X 528 X	1024 1024 96 1056 1056	600 ns 4095 4095 4095 4095 4095 4095 4032 4032	<pre>( 4160 ( 64 ) 64 ) 160 ) 4162 ) 4162 ) 466 ) 466</pre>	1, 800 ns 4224 128 128 176 4228 (132	_ □ 7 000.000 ns ↓ ↓ ↓ ↓ ↓ 4352 ↓ 256 ↓ 192 ★ 4360 ★ 264 ↓ 8
711alaw_tb_time_impl.wcfg Name Na	Value         0           0         0           0         0           1         0           156         0           192         4360           1352         0           192         0           4360         0           1         0           264         0           8         00	ns 0 X 0 X 1 X 1 X	64 ( 64 ( 32 ( 66 ( 2 (	0 ns 128 \ 128 \ 128 \ 132	256 256 64 264 8	00 ns   512 \ 512 \ 512 \ 512 \ 528 \ 528 \ 16 \ 100	1024 1024 96 1056 32	600 ns 4095 4095 (127 (4032 (4032 (63	<pre>(4160) (64) (64) (64) (64) (160) (4162) (66) (66) (160</pre>	1, 800 ns 4224 128 176 4228 132 4	— □ 7       000,000 ns       1 + 1 + 1
711alaw_tb_time_impl.wcfg Name Name Name Name Name Name Name Name	Value 0 0 1 4352 1 256 192 4360 1 264 8 100			0 ns 128 ( 128 ( 128 ( 128 ( 132	256 256 64 264 8	00 ns 512 X 512 X 512 X 528 X 528 X 16 X 100	1024 1024 96 1056 1056 32	600 ns 4095 4095 4095 4095 4095 4095 4032 4032	<pre>( 4160 ( 64 ) ( 64 ) ( 64 ) ( 160 ) ( 4162 ) ( 4162 ) ( 66 ) ( 2 ) /pre>	1, 800 ns 4224 128 128 176 4228 (176 4228	_ □ 7 000.000 ns ↓ 1 1 1 ↓ 4352 ↓ 256 ↓ 192 ↓ 4360 ↓ 264 ↓ 8
711alaw_tb_time_impl.wcfg Name Na	Value     0       0     1       4352     1       1     256       192     4360       1     1       264     1       100     1	ns 0 \ 0 \ 1 \ 1 \ 1 \		0 ns 128 ( 128 ( 128 ( 132 ( 133	256	00 ns 512 ( 512 ( 512 ( 512 ( 528 ( 528 ( 528 ( 16 () 100	1024 1024 96 1056 1056 32	600 ns 4095 4095 ( 127 ( 4032 ( 63	<pre>\ 4160 \ 64 \ 160 \ 4162 \ 4162 \ 66 \ 2</pre>	1, 800 ns 4224 128 176 4228 132 4	□ 7       000,000 ns       1, 1, 1, 1       (4352)       (4352)       (256)       (192)       (4360)       (4360)       (264)       (8)
711alaw_tb_time_impl.wcfg Name Na	Value 0 0 0 4352 1 256 192 4360 1 264 8 100			0 ns 128 ( 128 ( 128 ( 128 ( 128 ( 132	256 256 64 264 8	00 ns 512 X 512 X 512 X 528 X 528 X 16 X 100	1024 1024 96 1056 1056	600 ns 4095 4095 4095 4095 4032 4032	<pre>(4160 (64) (64) (64) (160) (4162) (4162) (4162) (4162) (4162) (4162) (4160) (4160) (4160) (64) (4160) (416) (4160)</pre>	1, 800 ns 4224 128 128 176 4228 (132 132	_ □ 7 000.000 ns ↓ 1 1 1 ↓ 4352 ↓ 256 ↓ 192 ↓ 4360 ↓ 264 ↓ 8
711alaw_tb_time_impl.wcfg Name Na	Value       0         0       0         0       0         4352       1         256       0         192       4360         13264       0         264       0         100       0	ns 0 \ 0 \ 1 \ 1 \ 1		0 ns 128 ( 128 ( 128 ( 132 ( 132 ( 48 ( 132 ( 48 ( 132 ( 48 ( 132 ( 48 ( 132 ( 48 ( 132 ( 48 ( 132 ( 1)	256 256 256 256 264 264 8	00 ns 512 X 512 X 512 X 528 X 528 X 16 X 100	1024 1024 96 1056 1056 32	4095 4095 4095 (127 (4032) (63	<pre>\ 4160 \ 64 \ 160 \ 4162 \ 4162 \ 66 \ 2</pre>	1, 800 ns 4224 128 176 4228 132 4	□ 7       000,000 ns       1, 1, 1, 1       (4352)       (4352)       (256)       (192)       (4360)       (264)       (8)

**Fig. 8.3:** Simulation for g711alaw. The simulations shows the a-law encoding and decoding and the associate errors for a power-of-two input positive input sequence and a few negative inputs too. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 8.4 adpcm

/adpcm_tb/clk	0																				
<pre>/adpcm_tb/reset</pre>	0																				
- Input: $-$	n	0	200	1400	1600	1800	1000										Ϋ́ο				
Index table:			200		1000	1000	1000														
	47	0	)e	3 (1	5 ) <u>2</u>	4 32	(40	(44	(43	42	41	(40	39	38	37	36	35	34	42	48	47
🔶 /adpcm_tb/i_underflow	0																				
/adpcm_tb/i_overflow	0				_																
/adpcm_tb/sz_out	658	0	11	16 ]3	4	3 (15	<u>7 )337</u>	<u>)</u> 494	<u>1 (449</u>	1408	371	337	307	1279	253	1230	209	<u>,190</u>	<u>(408</u>	724	<u> </u>
- Predictor/decoder output:	77	0		12	Ye	3 100	a 1522	Yoge	1046	loor	1041	Yoos	1037	Yood	1022	¥100	2 074	100	1 645	Y_19	72
/adpcm_tb/p_underflow	0	0	+-			<u>ə 122</u>	<u> 1522</u>	190:	<u>, 1040</u>	1990	<u>, 1041</u>		1057	1995	1000	100	2 19/4	1000		7-10	_ <u>//2</u>
/adpcm_tb/p_overflow	0																				
	-72	0		1	70)3	07 37	1 278	(15	(-46	10	-41	),5	-37	1	-33	<u>)</u> -2	26	<u>)</u> o	-645	(18	ľ
— 4 bit ADPCM coding word: —																					
🔶 /adpcm_tb/s_out	1											┑ᆜ								──┤	
/adpcm_tb/y_out	8	7					),5	)0	)8	)0	8	)0	8	0	8		)0	)F	Æ	<u>)</u> 0	8
Now	050 ns	11111111	i li i i					400		111						200		u u d		1000	
Cursor 1	.00 ns	0.00 ns		2	JUINS			400	i ns			600	ns			800	ris			1000	) ris
							(	(a)													
							(	<u>(a)</u>													
adpcm_tb_behav.wcfg								Accession Second		inninninn					an an an an an an an an an an an an an a			server and a server a			1 X
<b>+</b>																			1,050	.000 :	ns ^
Rame Valu	0 ns			200	ns			400 1	ns	L .		600 1	ıs			800 :	ns			1,00	0
Q- 1/2 /adpcm_tb/reset 0																					_
Mpdre		0 2	00 X 4	00 1 60		00 1					1000						- <u>v</u>		0		
Index table:																					-
▲ W /adpcm_tb/i_out[7:0] 47		0	8	X 16	24	X 32 X	40	44 X	43 4	12 X	41 🔾 4	۱ <mark>۰</mark> X	39 🗎 3	88 X	37 X :	¥ X	35	34	42 X ·	48 X4	17
V /adpcm_tb/i_underflow 0								_													
Step size:																					-
		0	16	X 34 >	73	X 157 X	337 X 4	194 X	449 X 4	08 X	371 X 3	\$7 X	307 2	79 X	253 X 2	30 X	209 1	190 X	408 X 7	724 X	
Predictor/decoder output:																					
E 📲 /adpcm_tb/p_out[15:0] 72		0		X3D	93	229	522 X 9	985 X.	1046 🗙 9	90 X	1041 9	\$5 X.	1037 9	99 X	1033 1	<u>рг X</u>	974 1	000 🔨	645 X -	- 8 X	72)
/adpcm_tb/p_underflow 0								_								+					
Adpcm_b/p_overnow 0		0		X 170	307	371	278	15 X	-46 1		-41	s v	-37	1 X	-33 X	-2 X	26	ο X.	-645 X	18 X	
4 bit ADPCM coding word:					(	<u>, , , , , , , , , , , , , , , , , , , </u>				<u> </u>				<u> </u>		- ^		<u> </u>	<u></u>		
Un /adpcm_tb/s_out 1																					
adpcm_tb/y_out[3:0] 8			7			X	5 X	¢Χ	8 X	• X	8 X	φX	8 X	<u>• X</u>	8		0 X	fχ	e_X	φX	8)
<b>□</b> - <b>□</b> T[31:0] 50										50											
۰ × ۰	• •					11						icicicia	(astastas	(april)		(10)(10)					- F
							(	$\mathbf{b}$													
								0)													



Fig. 8.4: Simulation for adpcm. The ADPCM CODEC shows a compression to a 4 bit signal. The simulation shows the encoder  $(y_out)$  and the decoder  $(p_out)$ . A fast triangular ramp is followed by a constant 1000 value to demonstrate the reduced quantization error with adaptation over time. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

### 8.5 pca

♦ /pca_tb/clk	0								
🔶 /pca_tb/reset	0								
➡─� /pca_tb/addr	1068								
💶 🤣 /pca_tb/data1	0000	028F				0000			
🛨 🔶 /pca_tb/data2	0000	0000				199A			<u> </u>
Input Data:									
🖅 🔶 /pca_tb/s1_in	0000 <del>4</del> 000		-++-+-+		++++++		++++++		
🖃 🔶 /pca_tb/s2_in	00000000								
₽-� /pca_tb/mu1_in	0				and the second s				
	0								range and the second second second second second second second second second second second second second second
Capas.									
₽-今 /pca_tb/w11_out	64186								
₽-� /pca_tb/w12_out	-12903								
∎-� /pca_tb/w21_out	12729								
₽-◆ /pca_tb/w22_out	64122					$\checkmark$			
	11120372								
Now	420 us	00 us 50	us 100	) us 150	us 200	) us 250	us 300	us 350	us 400 us
🗟 🎢 😑 🛛 Cursor 1	.00000 us	0.00000 us							
				(a)					

### Xilinx HDL Manual

→∏					
					420.000000 us
Name Name	Value	10 us	1100 115	1200 115	1300 us 1400 u
Q+ 10 (nca th/clk	0				
Q- 1% /pca_tb/reset	0				
	1068				
[] [] [] [] [] [] [] [] [] [] [] []	0000	0655			0000
Image: A state of the state	0000		0000	6554	0000
🖣 🖬 🖏 /pca_tb/s1_in[31:0]	00004000				
III III /pca_tb/s2_in[31:0]	00000000				
·순 속					
2 *** /pca_tb/mu1_in[31:0]	0000000				
↔ <b>// ¤ **</b> /pca_tb/mu2_in[31:0]	0000000				
<b>¤</b> -₩ /pca_tb/w11_out[31:0]	64186				
🛚 📢 /pca_tb/w12_out[31:0]	-12899				
🛚 🖬 /pca_tb/w21_out[31:0]	12730			-	
n dilam thung autorial	64124				
manna /pca_m/w22_out[31:0]	64134				
E - ₩ /pca_tb/x1_out[31:0]	fffe8372				
	000029e7				
<b>छ-₩</b> /pca_tb/y1_out[31:0]	ffffd749				
11 / /pca_tb/y2_out[31:0]	ffffd75c				
<b>⊞</b>	0000064	<u> </u>		0000064	
4			111		
	-   P		*** đ		



**Fig. 8.5.1:** Simulation for pca. The overall learning behavior of the principle component analysis (PCA) is shown. The first PC is learned when mu1 is active. The second PC is learned during the time mu2 is active. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The Verilog timing simulation does not match the behavior during the learning of the second PC.

<pre>/pca_tb/clk //pca_tb/reset</pre>	0	սուրուսուրուսիսուսիսուս
Testbench File Data:		
+	102C	
+	0000	
📕 🧄 /pca_tb/data2	0000	0000
Input Data:		
<b>- A</b> have the last in	55550000	
+	FFFFC000	
·	0	
	00000000	
+	00000000	0000000
Outputs:		
+	64186	64186
💶 - 🔷 /pca_tb/w12_out	-12903	-12903
🛨 /pca_tb/w21_out	12729	12729
🛨 /pca_tb/w22_out	64122	64122
Image: Provide the mathematication in the mathematication in the mathematication is a second sec	FFFEE372	[FFF X X X )FFFE X )0001 X )FFF X )000 X X X )000 X )FFF X )000
	27110	[ <u>10726 ]                                   </u>
	-76683	
	12376	
	12370	
<b></b>		
Now	420 us	410 us 411 us 412 us
Cursor 1	414 us	
		(a)

pca_tb_behav.wcfg	×
Name Value	410 us  411 us  412 us  413 us  414
Q+ 10. /pca.tb/dk 0	
Q- 1% /pca_th/reset 0	
Input Data:	
↓ □ ↓ /pca_tb/addr[12:0] 1068	
📉 🖭 📲 /pca_tb/data1[15:0] 0000	
I main and the second seco	0000
12	
🖆 ⊞ 📲 /pca_tb/s1_in[31:0] 16384	
4	
E.	
[↔] ፹ ☜ /pca_tb/s2_in[31:0] 0	
<u>KIL</u>	
□ ····································	00000000
	C 196
m /pca_b/w11_00t[31: _012800	
<pre>pca_ab/w12_out[31: 12239</pre>	
□ ₩ /pca tb/w22 out[31: 64134	64134
■ ₩ /pca tb/x1 out[31:0] fffe8372	
Image: Image	
	<mark>╶┼<sub>╧</sub>┙╴┝╴╺╫╴╘╴╶╢╘╴╶╛╺┱┟┥╘╴╶╛╴╫╴</mark>
🖬 📲 /pca_tb/y2_out[31:0] -10404	
<b>1</b> - <b>1 1 1 1 1 1 1 1 1 1</b>	00000064
	30

		(b)
pca_tb_time_impl.wcfg		×
20		
Name	Value	410.500 ns  411.000 ns  411.500 ns  412.000 ns  412.500 ns  413.000 ns  413.500 ns  414.
Qt 1‰ /pca_tb/dk	0	
🔍 🖓 /pca_tb/reset	0	
Input Data:		
Mathematical products of the second seco	16384	
<pre>pca_tb/s2_in[31:0]</pre>	-56756	<u>_X0X5X0X_56X0X5X0X_56X0X\$X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X0X5X0X_56X</u>
pca_b/mu1_in[31:0]	0	
Cutputs		
主 🖬 📲 /pca_tb/x1_out[31:0]	72688	<pre>\</pre>
🚛 🖽 /pca_tb/x2_out[31:0]	-27075	
	64186	64186
<pre>/pca_tb/w12_out[31:0]</pre>	-12899	
	-74790911	-747909114
21	/ ////	
1000		
	76518	┢╧╾┶╫╴┍╧╶┼┶┑╶┍╝╴┶┑╶┟╧╶┶┧╴┍╛╴╫╸
	45884072	┢┶┲╼┙┥╴┶┱╼┼┙╴┶┱┼┲┍╴┙┙╎┶┍╼┰┥╴
	100	
		(C)
Fig. 8.5.2: Simula	tion fo	r pca. Values after convergence. The 2 system outputs "y" should give a good
·	.1 0	

approximations to the 2 input signals "s". (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The simulation in (a,b) shows convergence in both signals, however, simulation (c) does not converge for the second PC.

### DSP with FPGAs/4e

### 8.6 ica

<pre>/ica_tb/dk</pre>	0	
<pre>//ca_tb/reset Testbench File Data:</pre>	0	
<b>⊡-</b> 今 /ica_tb/addr	12C	
	0000	
unput bata: ∎ /ica_tb/s1_in	0	
₽ <mark></mark>	16384	
₽-◆ /ica_tb/mu_in	0	
Outputs:      Outputs:      Ica tb/x1 out		
	FF	A COMPACING COMPACING COMPACING COMPACING COMPACING COMPACING COMPACING COMPACING COMPACING COMPACING COMPACING
	FF	
$+ - $ /ica_tb/B12_out	FF	
/ica_tb/B22_out	00	######################################
∎–今 /ica_tb/y1_out	74395	ᡧᢆ᠋ᢂ᠋ᡎᠧᢞ᠋ᡵᢥᡧᡎᡄᢞ᠊ᠾᢂᡧᡗᡇ᠕ᡧᡧᡎᠻᢢ᠋ᢤᡧᡁ᠕ᠰᡧᡀ᠕ᠰᠰᠰᡀᡀᡀᡀᡀᡀᡀ
₽-今 /ica_tb/y2_out	59987	
Now	30 us	
Garage Cursor 1	)00 us	00 us 5 us 10 us 15 us 20 us 25 us 30 us 0.00000 us
		(a)



### **DSP** with FPGAs/4e



**Fig. 8.6:** Simulation for ica. The ICA system learns faster and is more robust than the PCA system. Already after 20  $\mu$ s the 2 output signals y1 and y2 are good approximations to the input signals s1 and s2. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

# Chapter 9

#### 9.1 reg\_file



reg_file_tb_time_impl.wcfg						@ ×
20						1,000.000 ns ^
Name Name	Value	0 ns .	200 ns .	400 ns .	600 ns .	800 ns .
Image: A contract of the second se	)					
/reg_file_tb/reset 0	)					
S 1 /reg_file_tb/reg_ena 1	1					
Image: white the state of the sta	)		<u>    1                                </u>	3 0	1 2	3 0
Teg_file_tb/data[7:0] 1	16		<u>2</u> <u>4</u>	<u>    6                                </u>	<u>    10                                </u>	<u>14   16  </u>
→ ₩ ₩ /reg_file_tb/s[7:0] 4	4			2	4	
		<u>~</u>	^			
📲 🖬 📲 /reg_file_tb/rt[3:0] 3	3			3		
	14		0	X	6	14
<b>→ T</b> [31:0]	100			100		
				ļ		
\$1						~
:	$\langle \rangle$	<				>
			(c)			

**Fig. 9.1:** Simulation for reg\_file. First a normal write operations is shown. Register 0 is always 0. Registers 1,2, and 3 store the values 2, 4, and 6, respectively. Then with reg\_ena low registers 1 and 2 do not change values. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation. The local variable "r" is not available in the timing simulation.

#### 9.2 trisc0

<pre>/trisc0_tb/clk</pre>	0	ய	ļuu	hu	nur	LUU	Γſ	ГЛ	L.	ЛЛ	hu	hun	hu	hu	hu	hur	hu	nn
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### **Xilinx HDL Manual**

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**Fig. 9.2:** Simulation for trisc0. The trisc0 is a stack machine that comes with a basic C-compiler and assembler program. The simulation shows the computation of a factorial for 3, i.e. 2\*3=6 done in a loop. I/O ports are used to specify the factorial argument (iport) and the LEDs (oport) are used to display the result. (a) VHDL ModelSim simulation. (b) Vivado Verilog behavior simulation. (c) Vivado Verilog timing simulation.

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