Lastname: ___________________

5Digit SS:___________________

LABORATORY
Number Systems and Quantization

LAB : NUMBER SYSTEMS AND QUANTIZATION
(10 points)

In this lab you will be introduced to fractional number systems.
In the **pre-lab** you will compute via "pencil-and-paper" the results you later expect in your design implementation. In the **design part** you will design and simulate a 5-bit bus implementation of a fractional number system.

Lab Objectives

After completing this lab you should be able to:

- Understand the difference between signed and unsigned numbers systems
- Determine the minimum and maximum values that can be represented in integer and fractional number systems
- Compute quantization error
- Design and simulate a circuit using Simulink

Pre-lab (3 points)

1. Our board uses an **unsigned** 12 bit A/D converter.

   a. Determine the minimum number that can be represented by the A/D converter:

   X_{min} = ___________________

   b. Determine the maximum number that can be represented by the A/D converter:

   X_{max} = ___________________

2. Suppose that, instead, we used a **signed** 14 bit A/D converter in our board.

   a. Determine the minimum number that can represented by the A/D converter:

   Y_{min} = ______________________

   b. Determine the maximum number that can be represented by the A/D converter:

   Y_{max} = ______________________

3. For signed fractional numbers with 3 integer and 2 fractional bits (Xilinx `Fix_5_2` format).

   a. determine the decimal weight (+/-2^k) for each digit:

      _____________ . ______________

   b. determine, in binary format, the largest positive number that can be represented:

      B_{max} = ___________

   c. determine the equivalent of B_{max} as a decimal number:

      D_{max} = ___________

   d. determine, in binary format, the smallest positive number that can be represented:

      $B_{smallest}$ = ___________

   e. determine the equivalent of $B_{smallest}$ as a decimal number:

      $D_{smallest}$ = ___________

   f. determine, in binary format, the minimum negative number that can be represented:

      B_{min} = ___________

   g. determine the equivalent of B_{min} as a decimal number:

      D_{min} = ___________

4. Complete the table below for the `Fix_5_2` format with **Quantization: Truncate**

Decimal Value	**Binary** `Fix_5_2` **format**	**Decimal** `Fix_5_2` **equivalent**	**Quantization error (Dec. equivalent-Dec. Value)**
2.5			
-1.75			
1/8			
7/3			
D_{max} =			
D_{max} + D_{min} =			

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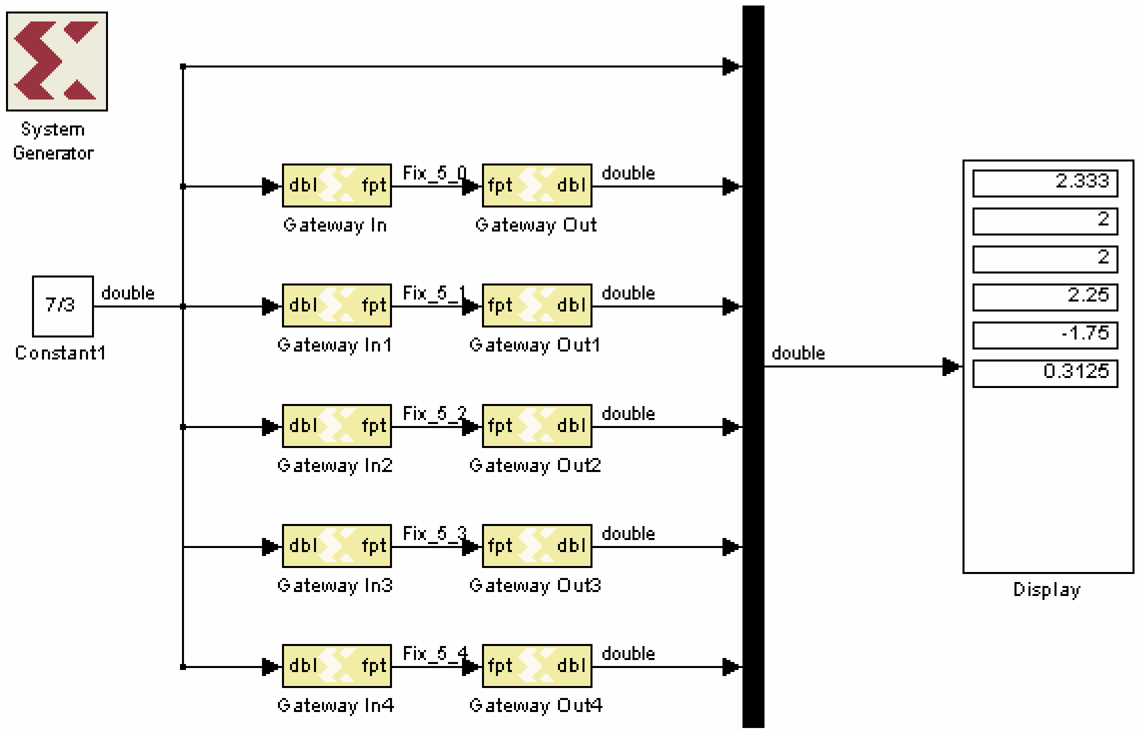
LABORATORY
Number Systems and Quantization

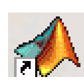
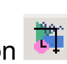
Simulink Design-lab

Follow the directions below to implement the following circuit



A. Getting Started

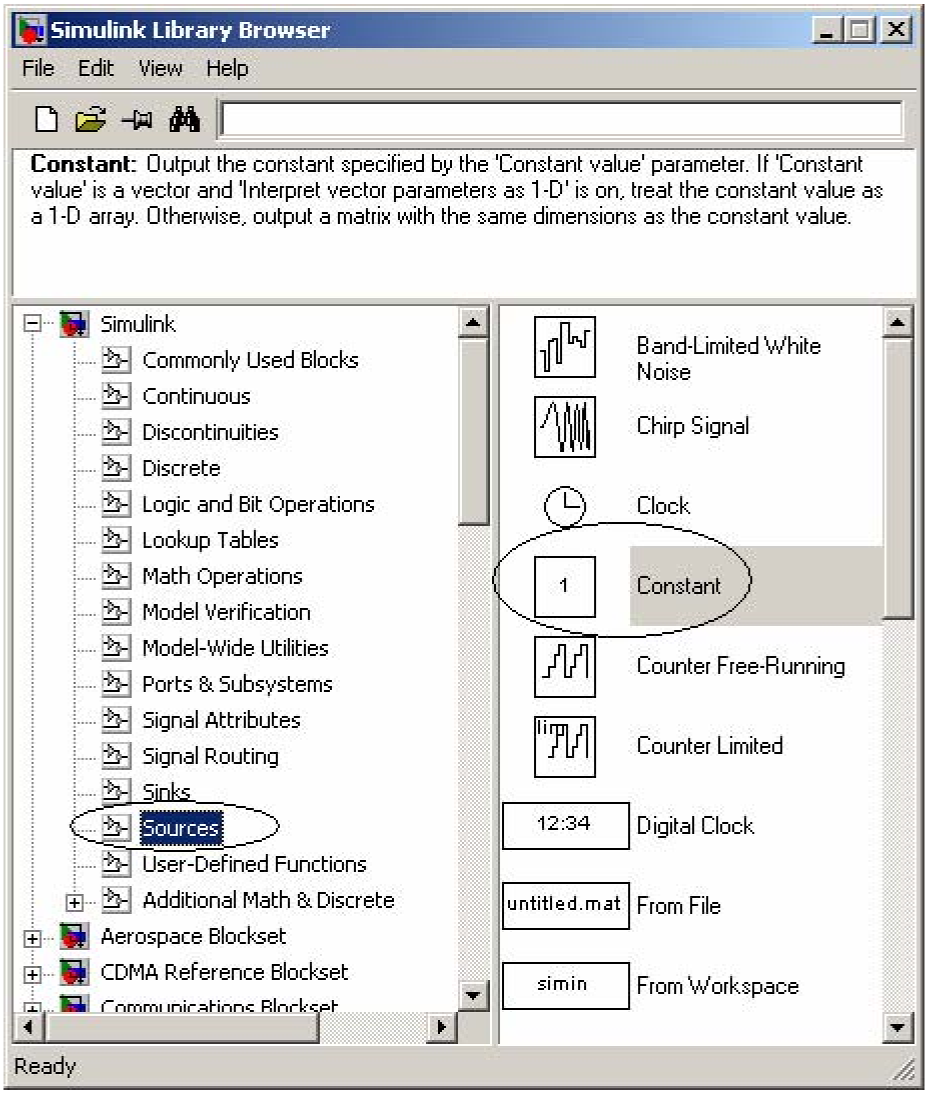
If you are in room B114 or the digital logic lab:

1. On the desktop, double click on the **Engineering Folder**.
2. Double click on the MatLab icon  to start MatLab. It will take a few seconds to load.
3. From the top icon list in the **MatLab** window click on the **Simulink** icon  to start **Simulink.**
4. Create a New Folder on your mapped network drive and name it **DSPwFPGAs.** Use this folder to save your designs. **Never** save your files to the local drive, use your **network drive** or a **USB drive** instead**.**

B. Creating Your Simulink Design

1. Select **New Model** from the **File** menu or click on the **New Model** button in the **Simulink Library Browser**.
2. Save your design using **Save as** from the **File** menu. Remember to save often as you complete your design.

3. From the **Simulink Library Browser,** choose the **Simulink** library and click on **Sources**. Choose the **Constant** source block and drag it into your worksheet, or click on the block and use **CTRL+I** to add it to the worksheet automatically.

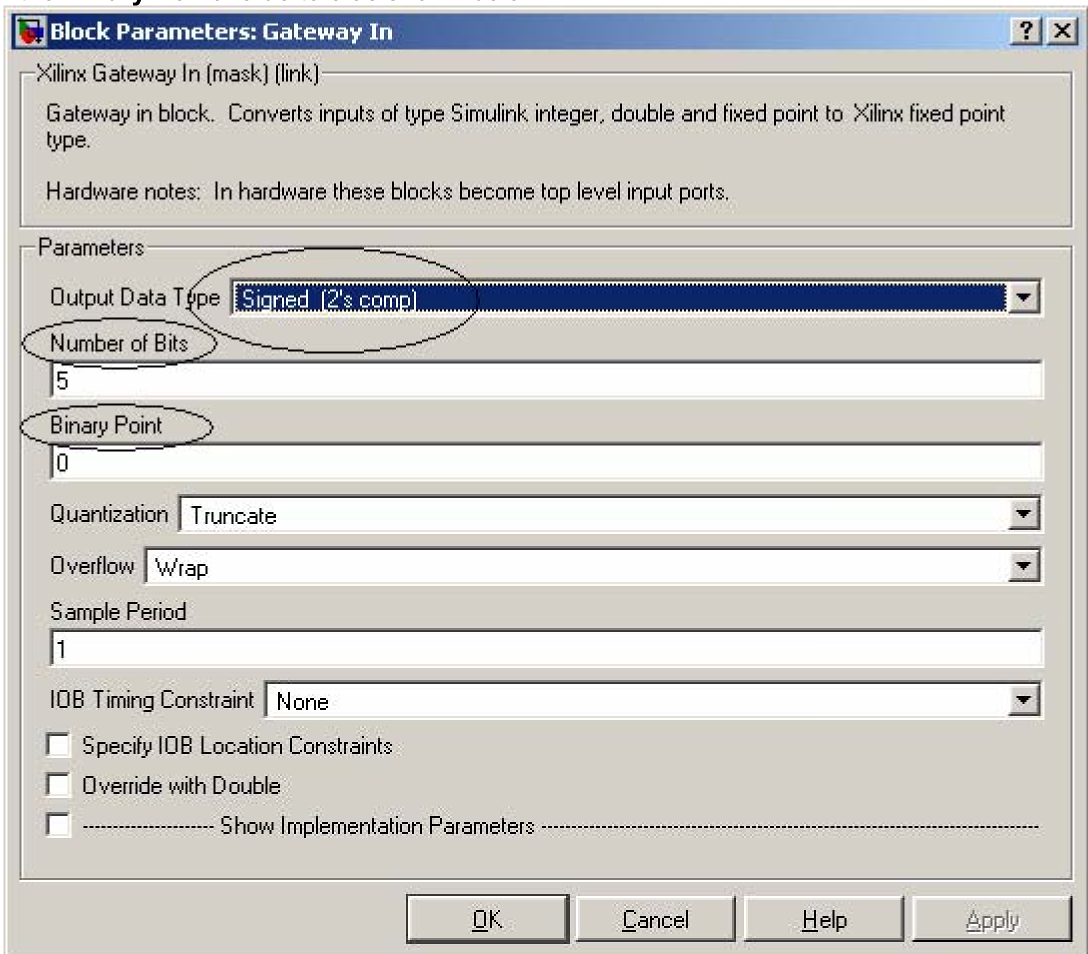


4. To change the **Constant** source's value to 7/3, double click on the **Constant** source block and Type 7/3 for the **Constant Value** field.

5. To add the Gateways (inputs and outputs), go to the **Xilinx Blockset** library, then **Basic Elements**. Choose the **Gateway In** block and place 5 of them in your worksheet, or add one **Gateway In** block and use **Copy & Paste** to add the remaining 4 Gateways. Repeat this process for the **Gateway Out** blocks. Note that the **Gateway Out** modules must be added to the design because the Display, or any other Simulink block, cannot connect directly to Xilinx blocks unless they first pass through a **Gateway In** or **Gateway Out** module, due to data formats incompatibility.

6. Wire the **Constant** source to each of the input gateways by connecting wires from the output of the source to the input gateways. This can also be done by clicking on the source, pressing **CTRL** and then using the mouse to left click on the input gateways.

7. To change input gateway configuration, double click on one of the **Gateway In** blocks. Change the **Output Data Type** to Signed (2's comp). Then change the **Number of Bits** value to 5 and the **Binary Point** value to 0 as shown below.



8. Repeat the previous step for the remaining input gateways, selecting 5 for the **Number of Bits** of each gateway. Set their **Binary Point** value to 1, 2, 3 and 4 respectively.

9. Under the **Simulink** library, go to **Signal Routing** and add the multiplexer (**Mux**) to your design. Note that this is the Simulink multiplexer, **not** a Xilinx block.

10. In your design, double click on the multiplexer icon and change the **Number of Inputs** to 6. You can change the size of the multiplexer by clicking on it, placing the cursor on one of the corners and dragging the double-ended arrows.

11. Connect the **Constant** source to one of the multiplexer inputs and the **Gateway Out** blocks to the remaining multiplexer inputs.

12. Go to **Sinks** in the **Simulink** library and add the **Display** block to your design.

13. Wire the **Display** to the output of the multiplexer.

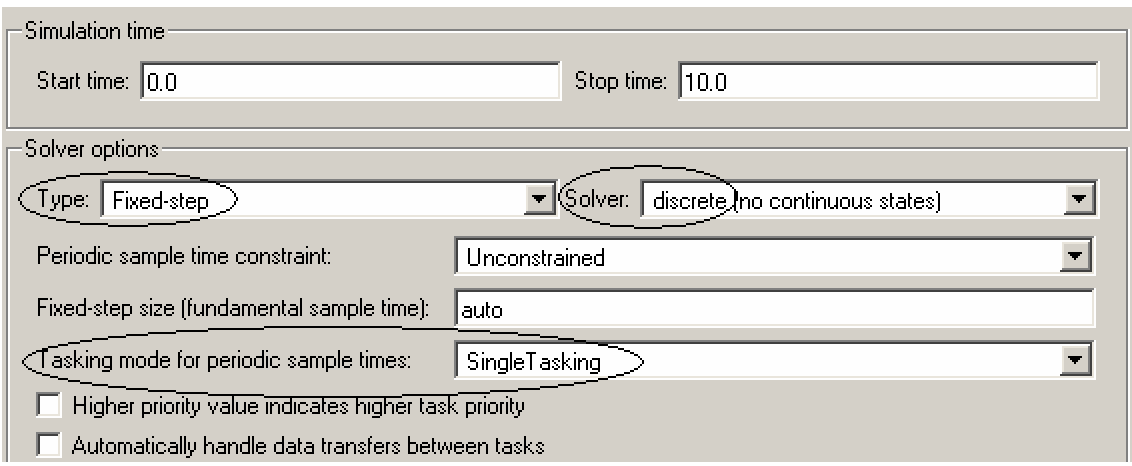
14. Enlarge the **Display** icon so the values of all outputs can be seen after simulation.

15. Finally, under the **Xilinx Blockset,** go to **Basic Elements** and add the **System Generator** block to your design. Remember that, without **this block**, you **won't** be able create your project files or simulate your design.

C. Simulating your Design

1. On the menu bar, go to **Simulation** and click on **Configuration Parameters,** or use **CTRL+E**. Choose the following configuration parameters:

   Type: Fixed-step
   Solver: discrete (no continuous states)
   Tasking mode for periodic sample times: single tasking



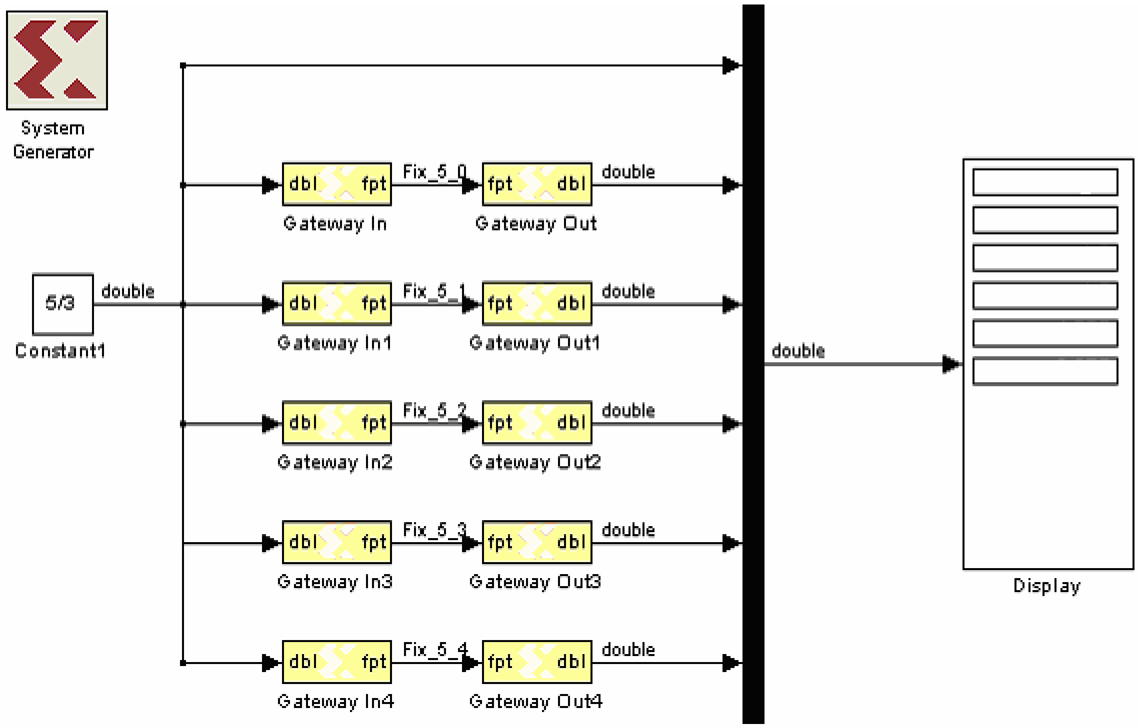
2. On the menu bar, go to Format, Port/Signal Display and make sure Port Data Types is checked. This way, Simulink will show the data types leaving each block. This can be very useful when "debugging" a larger design.

3. To simulate your design, click on the **Start Simulation** button, choose **Start** under the **Simulation** menu, or use **CTRL+T**.

4. Repeat the previous step for a **Constant Value** of 5/3, and fill out below the empty scope with your results.

5. Complete the following table for values close to the boundary conditions for the `Fix_5_2` format with **Quantization: Truncate.** Compare your results with the pre-lab data.

Constant Value	Display	Error (Display-Value)	Overflow (yes/no)
3.75			
4.0			
-4			
-4.25			



D. Deliverables:

1. Solve the problems from the pre-lab. (3 points).

2. Print the MDF file (after simulation with 5/3 constant). (7 points)

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