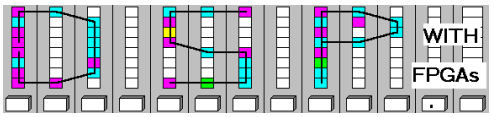
Lastname: _____

5Digit SS:_____

LABORATORY
Into. Simulink+ Xilinx
System Generator



LAB : INTRODUCTION TO SIMULINK AND XILINX SYSTEM GENERATOR
(10 points)

In this lab you will be introduced to the Simulink environment for the Digilent's Nexys Development board. In the **pre-lab** you will compute with "pencil-and-paper" the results you later expect in your design implementation. In the **design part** you will complete the design of a sine wave generator and become comfortable with the Simulink and Xilinx ISE environment.

Lab Objectives

After completing this lab you should be able to

- Associate components with their library
- Understand the Simulink/System Generator design flow
- Design and simulate a circuit using Simulink

Pre-lab (3 points)

1. Download the board documentation for the Nexys Development board and the FPGA's datasheet from the course webpage and answer the following questions.

   a. What is the exact name of the FPGA on the board? _____

   b. How many (equivalent) logic cells does the FPGA has? _____

   c. How many embedded multipliers are on the FPGA? _____

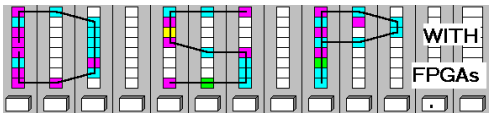
   d. How many 18KBits embedded BlocksRAMs does the FPGA has ? _____

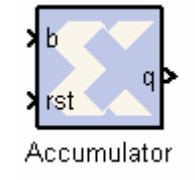
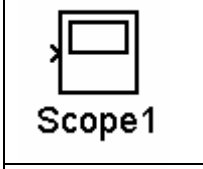
   e. Suppose jumper JP4 is open. What is the input frequency to the FPGA? _____

   f. Determine the pin location of BTN0= _____, SW0=_____, and LD0=_____.

2. For the following elements, determine the library name and subgroup of the library:

Element	Directory	Sub-directory
 System Generator		



3. A function generator uses a LUT to store a sine table. The input to the function generator is a triangular signal, and the output an unsigned sine wave. Complete the following, assuming the frequency of the sine wave is desired to be 50 kHz and the triangle function is generated with an accumulator (increment M) running at 50 MHz and B=29 bit width.

   a. Determine the period length of the 50 kHz sine wave:

      T =_____

   b. Determine M for a 14 bit accumulator with an output frequency of 50 kHz:

      M = _____

4. The sine frequency is, in general, too high to be seen on the 7-segment LEDs. If only the MSBs of a 29 bit accumulator are used for the LED display.

   a. Determine the LED period length for M=1 and a 29 bit accumulator:

      T = _____

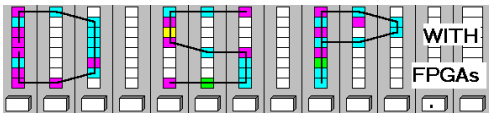
   b. Determine the period for a 14 bit accumulator with M =1

      T= _____

Lastname: _____

5Digit SS:_____

LABORATORY
Into. Simulink+ Xilinx
System Generator



Simulink Design-lab

Follow the directions below to implement your first circuit with Simulink

.

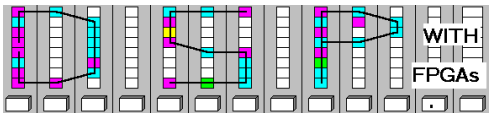
A. Getting Started

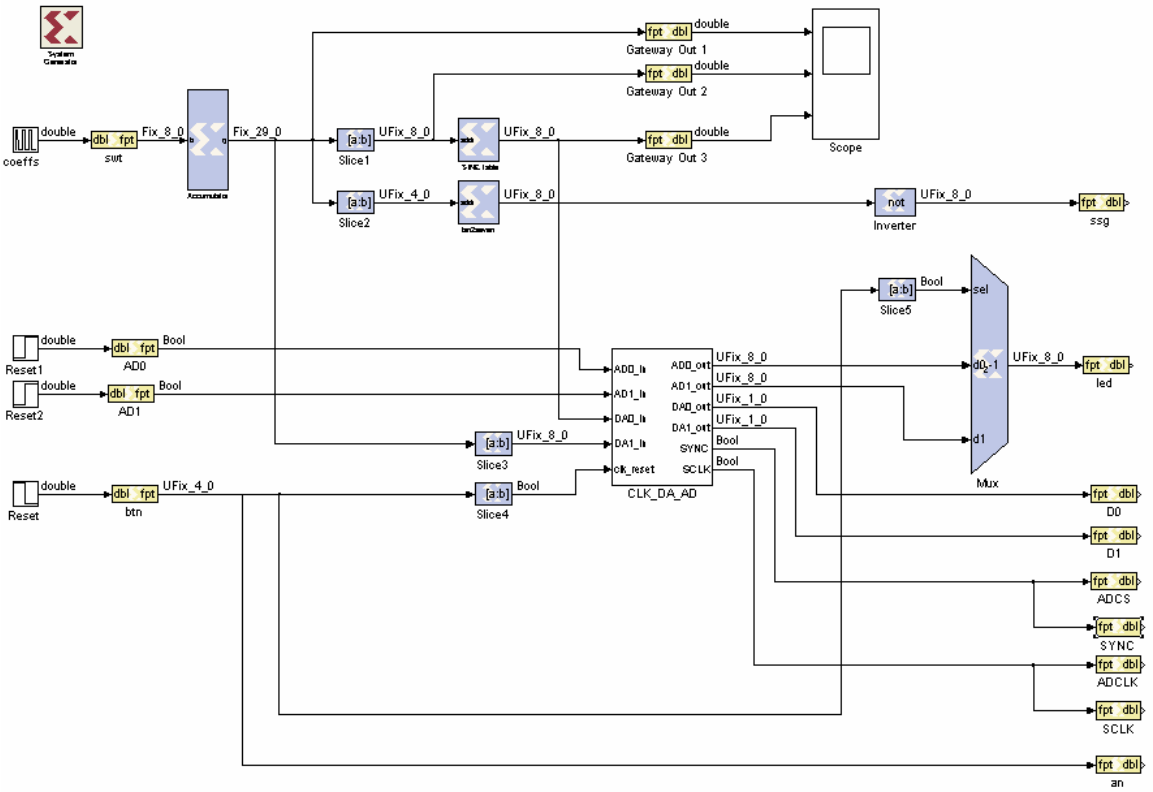
If you are in room B114 or the digital logic lab:

1. On the desktop, double click on the **Engineering Folder**.
2. Double click on the MatLab icon  to start MatLab. It will take a few seconds to load.
3. From the top icon list in the **MatLab** window click on the **Simulink** icon  to start **Simulink.**
4. Create a New Folder on your mapped network drive and name it **DSPwFPGAs.** Use this folder to save your designs. **Never** save your files to the local drive, use your **network drive** or a **USB drive** instead**.**

B. Compiling an Existing Design

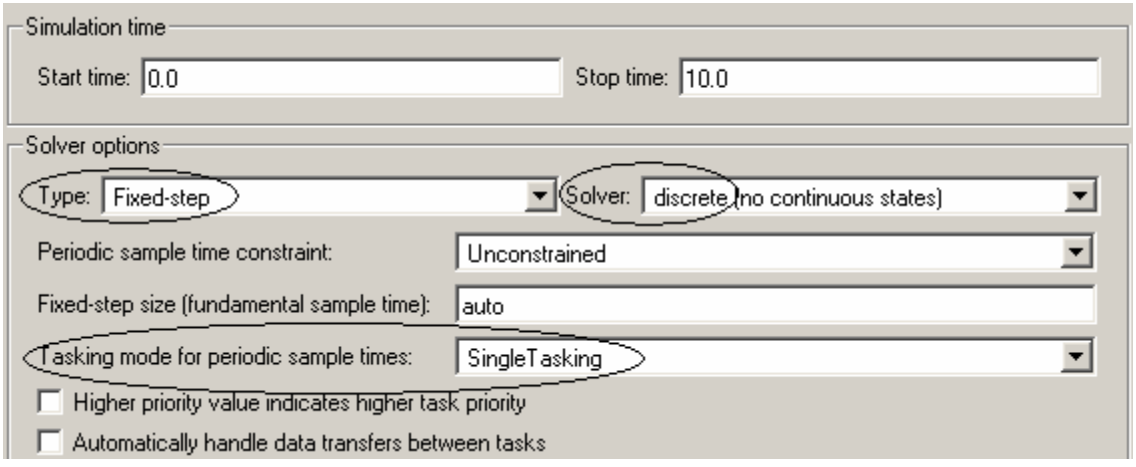
1. Download the files **lab1.mdl** and **lab1.ucf** from the class webpage into your **DSPwFPGAs** folder.
2. For convenience, in **MatLab,** click on the "Current Directory" selection icon  and select your **DSPwFPGAs** folder as the current directory.
3. In the **Simulink Library Browser** window, go to **File**, then **Open**. Go to your **DSPwFPGAs** folder and locate the file **lab1.mdl**. Double click on lab1.mdl to open it. After a moment, you should see a design like the one in the following figure.

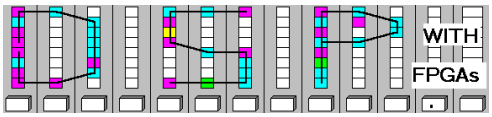




4. On the menu bar, go to **Simulation** and click on **Configuration Parameters,** or use **CTRL+E**. Choose the following configuration parameters:

   Type: Fixed-step
   Solver: discrete (no continuous states)
   Tasking mode for periodic sample times: single tasking

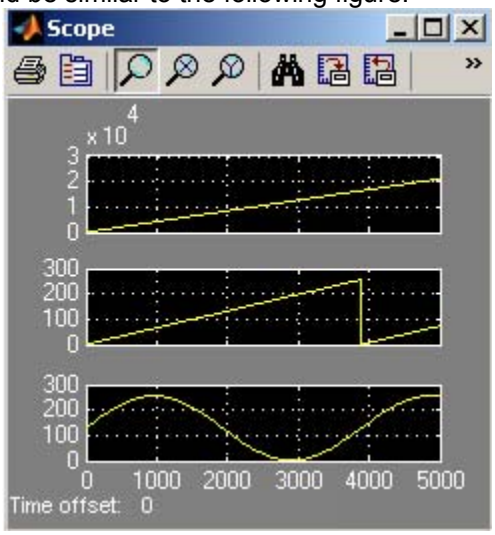




5. On the menu bar, go to **Format**, **Port/Signal Display**. Make sure **Port Data Types** is checked. This way, Simulink will show the data types leaving each block. This can be very useful when "debugging" a larger design.

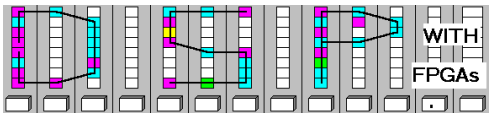
6. To simulate the design, click on the **Start Simulation** button, choose **Start** under the **Simulation** menu, or use **CTRL+T**.

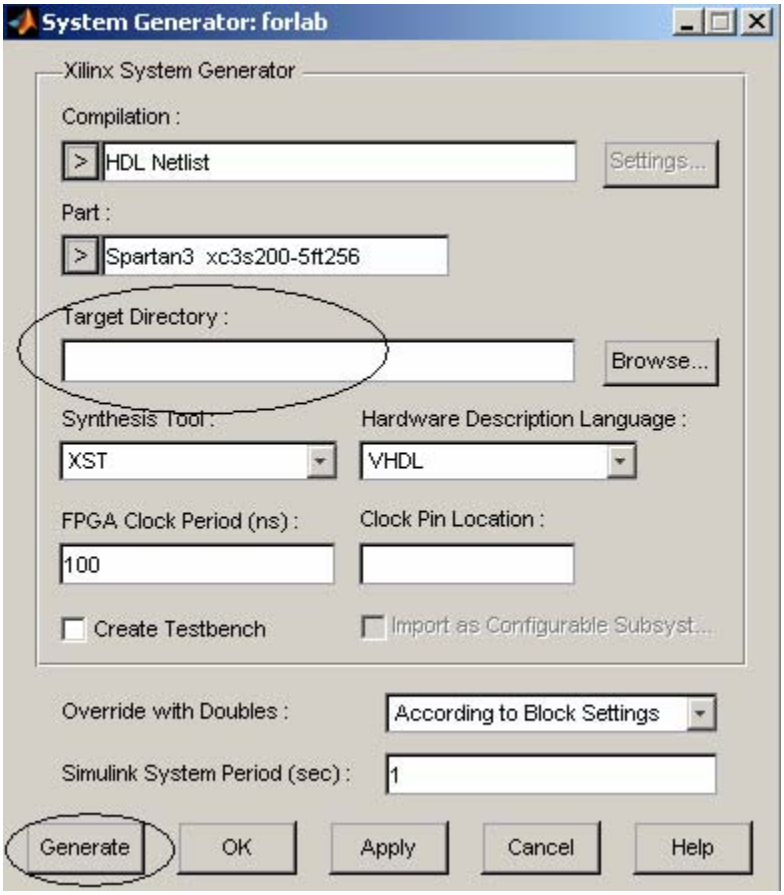
7. In order to see the output of the simulated scope double-click on the **Scope** block. A window should appear with three graphs, one for each input. Click the  icon to Auto scale all the graphs. The result should be similar to the following figure.



8. Next, double-click on the **SignalGenerator** block to create the design's project files.

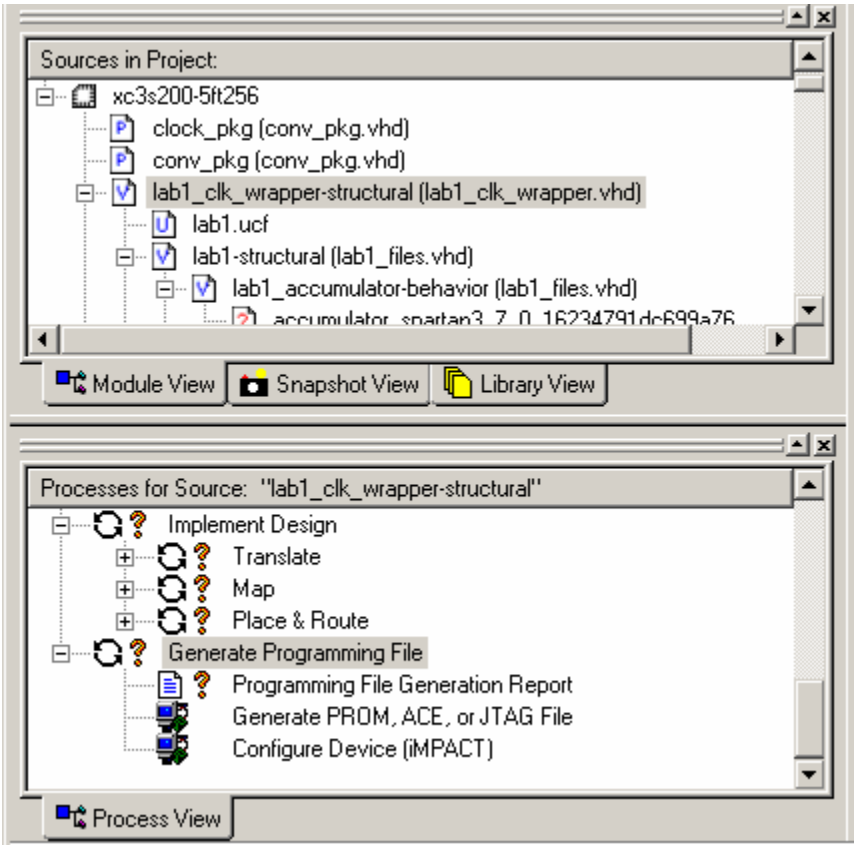
9. For the field **Target Directory,** click browse and set the target directory to your **DSPwFPGAs** folder. Then, click on the **Generate** button at the bottom of the window. This may take a few minutes.





10. Once the Generation is complete, there should be a Project File called lab1.ise in your **DSPwFPGAs** folder. Open **Xilinx Project Navigator** from the desktop icon or through the Windows start menu. Go to **File**, **Open**, then go to your **DSPwFPGAs** folder and double click on the **lab1_clk_wrapper.ise** file**.**

11. On the left you will see a window titled **Sources in Project**. Find the line containing the title **lab1_clk_wrapper-structural (lab1_clck_wrapper.vhd)**. Right click on this line and choose add source. In your **DSPwFPGAs** folder, select the file **lab1.UCF**. UCF files contain the pin assignments from the Gateway Out blocks that connect to the board. You may open **lab1.ucf** with a text editor to see the format of these pin assignments.



12. Now that the source is added, click on the **lab1_clk_wrapper-structural (lab1_clck_wrapper.vhd)** to bring up additional options in the lower left hand window titled **Processes for Source.**

13. In the **Processes for Source** window, scroll down and find **Generate Programming file**. Right click and select **Run**. This may take several minutes.

14. Determine the number of required 4-input lookup tables (LUTs), block RAMs, and embedded 18x18bit multipliers from **View Design Summary** and the maximum frequency from the **Post Place and Route Static Timing Report** under **Detailed Reports**.

4 input LUTs = _____

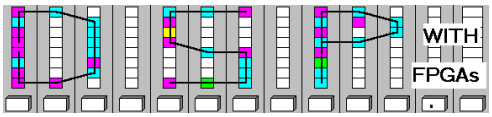
Block RAMs =_____

Multipliers 18x18s =_____

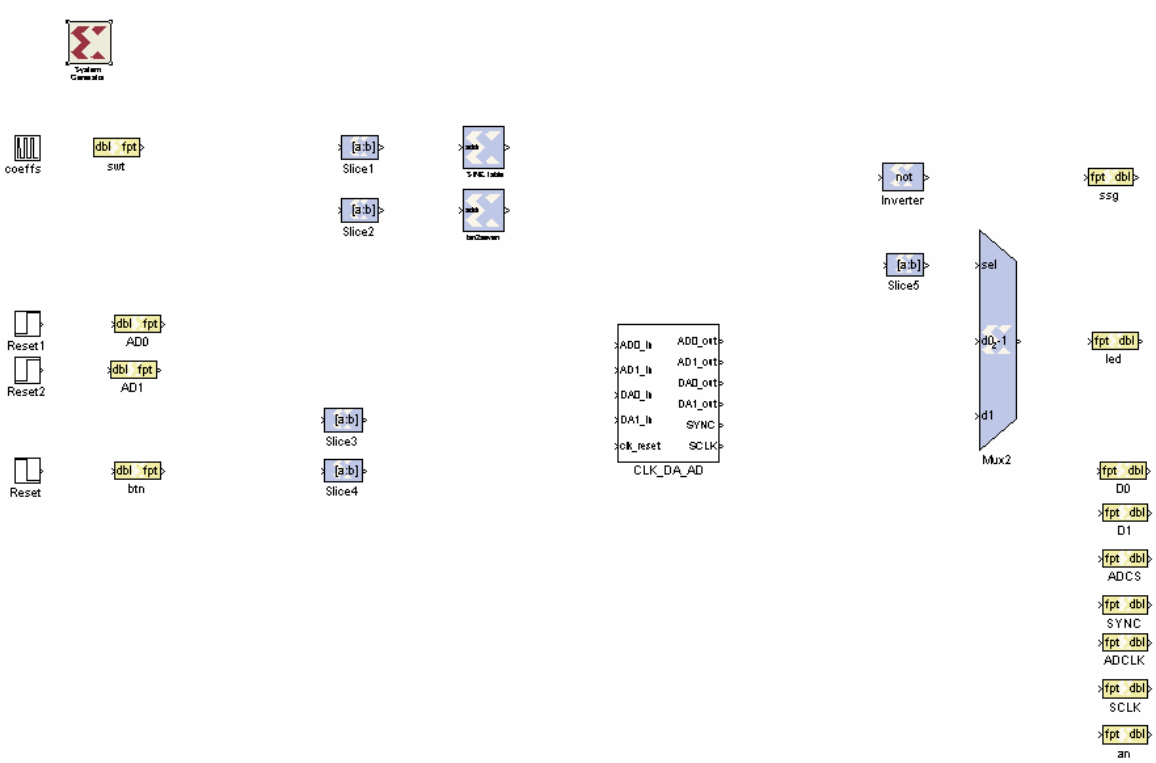
Max. Freq. = _____

C. Completing The Simulink Design

1. Download the file **lab1inc.mdl** from the class webpage into your **DSPwFPGAs** folder.



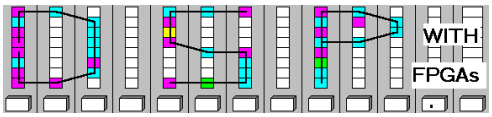
2. In the **Simulink Library Browser** window, go to **File**, then **Open** and find the file **lab1inc.mdl** which you just downloaded. After a moment you should see an incomplete design like the one in the following figure.

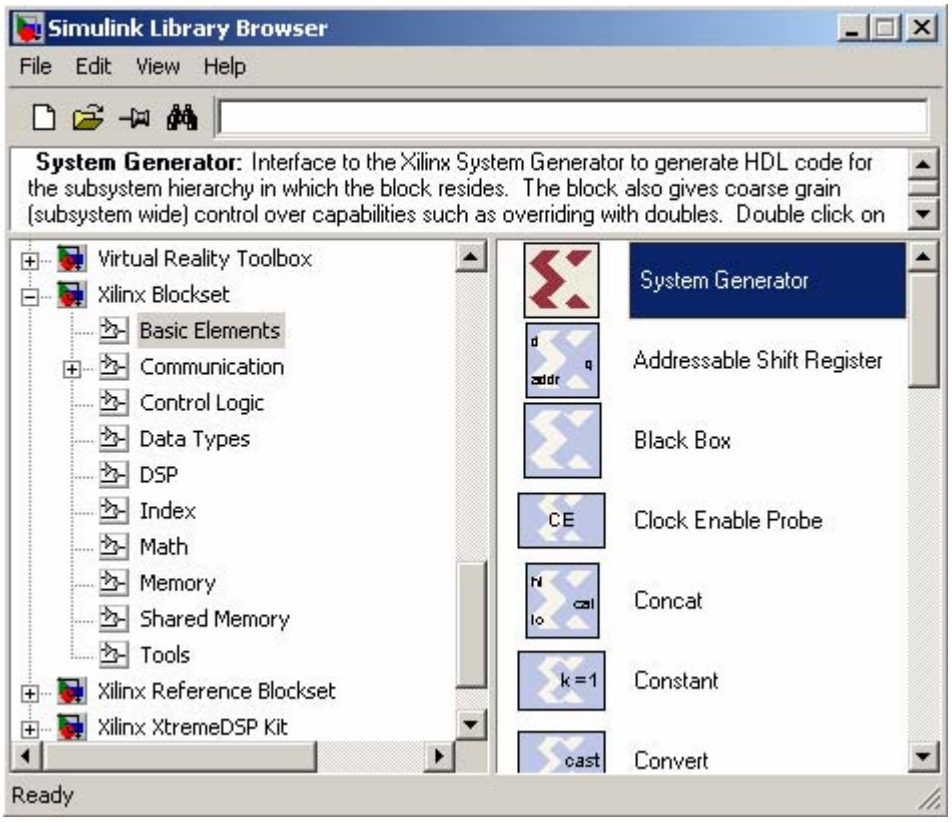


3. Begin completing the circuit diagram by adding the **SystemGenerator**. The System Generator block is needed to control the system and simulation parameters and is used to generate the project files.

   a. Go to the **Simulink Library Browser** window. If this window is not already open, select the **Simulink** icon  in **MatLab.**

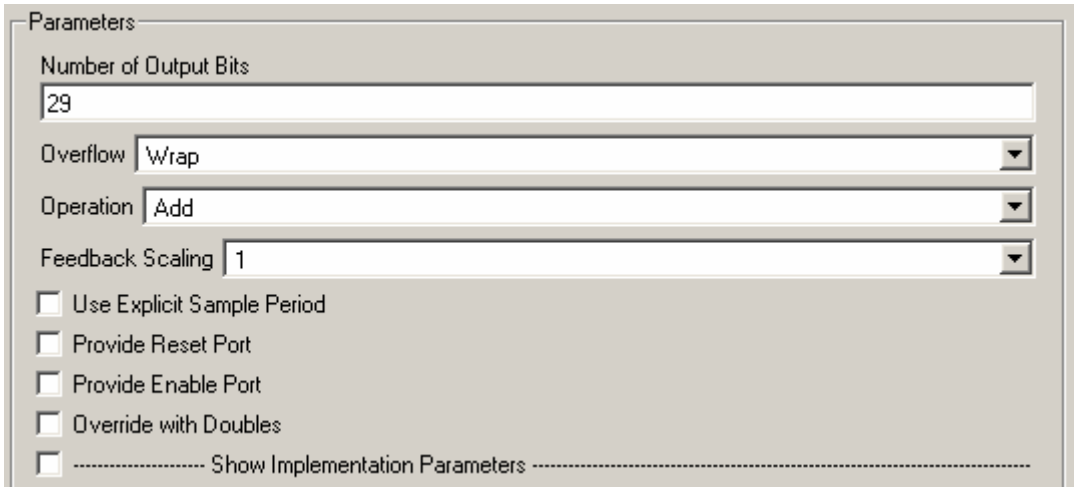
   b. On the left, there will be a list of blocksets. Scroll down and double click on **Xilinx Blockset**. A list of subdirectories will open underneath it and in the window to the right. Double click on the subdirectory **Basic Elements**. On the right, a list of blocks should appear along with the **SystemGenerator** block, as seen in the following figure.

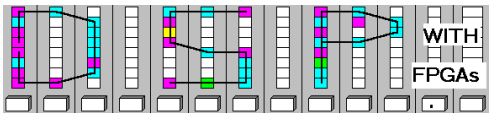




c. Drag the **SystemGenerator** block from the library window to your diagram.

4. Add and connect the **Accumulator** block.
   a. Find the **Accumulator** block in the **Simulink Library Browser,** under **Xilinx Blockset**, under the subdirectory **Math**.
   b. Drag the block to your diagram window beside the Gateway In block labeled **swt**. Note that the size of the blocks can be changed by selecting the block, then dragging the corner of the block to the desired size.
   c. Double-click the **Accumulator** block to view the settings and adjust them to match the figure shown below.





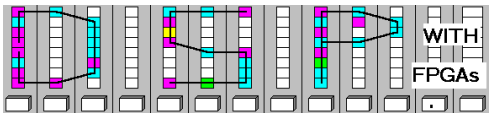
d. Click **OK** to save the parameters.
e. Next, connect the Accumulator to the Gateway In block. First, select the Gateway In block labeled **swt** by left-clicking on it. Now that the box is selected, press and hold the **Ctrl** key on your keyboard and select the **Accumulator** block. A wire should appear connecting the **swt** block to the **Accumulator** block**.**

5. Connect all the blocks that are floating. Blocks can also be connected by clicking on their inputs or outputs and dragging a wire to the desired connection point. Also, note that you can find generic information on a block by right-clicking on the block and selecting help.

   a. Start by connecting the **Source** blocks to the **Gateway In** blocks immediately to their right.
   b. Connect the **input** of the **Slice2** and **Slice3** blocks to the **output** of the **Accumulator**. (Note that you can not click and drag a wire from the Accumulators output since it is already connected to the Slice1 block.)
   c. Next, connect the **output** of the **Slice1** block to the **input** of the **SINE Table** block and the **output** of the **Slice2** block to the **input** of the **bin2seven** block.
   d. Using whichever method you prefer, connect the **bin2seven** block to the **Inverter** block. Then, connect the **Inverter** block to the **ssg** output block.
   e. Connect the **AD0** and the **AD1** input blocks to the inputs of the **CLK_DA_AD** block labeled **AD0_in** and **AD1_in,** respectively.
   f. Next, connect the **input** of the **CLK_DA_AD** block labeled **DA0_in** to the **output** of the **SINE table** block and connect **DA1_in** to the **Slice3** block.
   g. Connect the **btn** input block to the **Slice4** block, then connect the **Slice4** block to the input of the **CLK_DA_AD** block labeled **clk_reset.**
   h. Now, Connect the **input** of the **Slice5** block to the output of the **btn** input block, then connect the **output** of the **Slice5** block to the **input** of the **Mux** block labeled **sel**.
   i. Next, connect the **outputs** of the **CLK_DA_AD** block labeled **AD0_out** and **AD1_out** to the **inputs** of the **Mux** labeled **d0** and **d1** respectively.
   j. Now, connect the **output** of the **Mux** to the **led** output block.
   k. Connect the **input** of the **an** output block to the **output** of the **btn** input block.
   l. Connect the output of the **CLK_DA_AD** block labeled DA0_out to the D0 output block and the one labeled DA1_out to the D1 output block.
   m. Finish up by connecting the output to the **CLK_DA_AD** block labeled **SYNC** to **BOTH** the **ADCS** and the **SYNC** output blocks. Then connect the output labeled as **SCLK** to **BOTH** the **ADCLk** and **SCLK** output blocks.

6. **Save** your design to your **DSPwFPGAs** folder.

7. Your completed design should now look like the design opened at the beginning of this lab, with the exception of the scope.



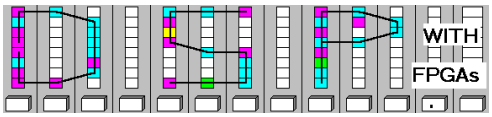
D. Simulating your design in Simulink

Since creating the project files, compiling the project files and downloading the design to the board can take a considerable amount of time, it is often the case that you'll want to simulate the output of the circuit. In this case, a simulated **oscilloscope** will be used to view the output at particular points of the schematic.

1. Add the **Scope** to the schematic.
   a. To add a scope, go to the **Simulink Library Browser** window which can be opened by clicking on the  icon in **MatLab**.
   b. In the left-hand window at the top, click on the **Simulink** directory, then go to the subdirectory called **Sinks**.
   c. Find the **Scope** block and drag it to your diagram window. Note that the scope only has one input, but we need three.
   d. To change the number of inputs to the scope, double-click on the **Scope** block to have the graph window pop up.
   e. At the top of the window, click the Parameters icon  .
   f. Change the number of axes to 3, as shown below.

   g. Click OK and close the graph window to return to your diagram window. You should now see three inputs into the **Scope**.

2. In order to connect to the **Xilinx** blocks to the **Scope** you will need a **Gateway Out** block for each input into the **Scope**. (Similarly, Gateway In blocks are needed for inputs to Xilinx blocks from non-Xilinx blocks.)
   a. Again, go to the **Simulink Library Browser** window.
   b. In the left-hand window click on the directory **Xilinx Blockset**, then go to the subdirectory **Basic Elements**.
   c. Find the **Gateway Out** Block and drag **Three** of them to your diagram window. (You may drag them one at a time or drag one and then copy and paste two more from it)
   d. Connect one of the **Gateway Out** blocks to the **output** of the **Accumulator** block.
   e. Connect one of the **Gateway Out** blocks to the **output** of the **Slice1** block.
   f. Connect one of the **Gateway Out** blocks to the output of the **SINE table** block.
   g. Connect the **outputs** of each of the **Gateway Out** blocks to each of the **inputs** of the **Scope** block.



3. To simulate your design, click on the **Start Simulation** button, choose **Start** under the **Simulation** menu, or use **CTRL+T**. Make sure the simulation **Configuration Parameters** are the same as in part B

4. Double-click the **Scope** block. The scope window with three graphs should appear. Hit the  icon to Autoscale all the graphs. Verify that the scope displays two saw tooth waves and a sin wave as in part B.

E. Compiling Your Design using SignalCompiler

This part of the lab is very similar to the procedures followed in Part B.

1. Double-click the **SignalGenerator** block.

2. For the field **Target Directory,** click browse and set the target directory to your **DSPwFPGAs** folder. Then, click on the **Generate** button at the bottom of the window.

3. Once the Generation is complete there should be a **Project File** called **lab1inc.ise** in your **DSPwFPGAs** folder. Open **Xilinx Project Navigator**  from the desktop icon or through the windows start menu. Go to **File**, **Open**, then go to your **DSPwFPGAs** folder and double click on the **lab1.ise** file**.**

4. On the left you will see a window titled **Sources in Project**. Find the line containing the title **lab1inc_clk_wrapper-structural (lab1inc_clck_wrapper.vhd)**. Right click on this line and go to add source. In your **DSPwFPGAs** folder, select the file **lab1.ucf**.

5. Now that the source is added, click on the **lab1inc_clk_wrapper-structural (lab1inc_clck_wrapper.vhd)** to bring up additional options in the lower left hand window titled **Processes for Source**.

6. In the **Processes for Source** window, scroll down and find **Generate Programming file**. Right click and select **Run**. This may take several minutes.

7. Determine the number of required 4-input lookup tables (LUTs), block RAMs, and embedded 18x18bit multipliers from **View Design Summary** and the maximum frequency from the **Post Place and Route Static Timing Report** under **Detailed Reports**.

4 input LUTs = _____

Block RAMs =_____

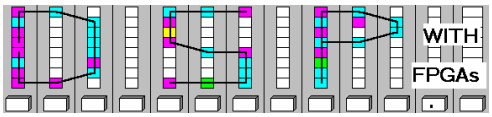
Multipliers 18x18s =_____

Max. Freq. = _____

F. Download your design to the FPGA board

Once you have completed the compiling process, you can download your design to the board. Make sure your computer has a board connected to it. If not, move to a computer that has a board.

1. A third program will be needed to actually download your programming file onto the board. Open the program **Ex-port** from either the desktop icon or through the windows start menu.



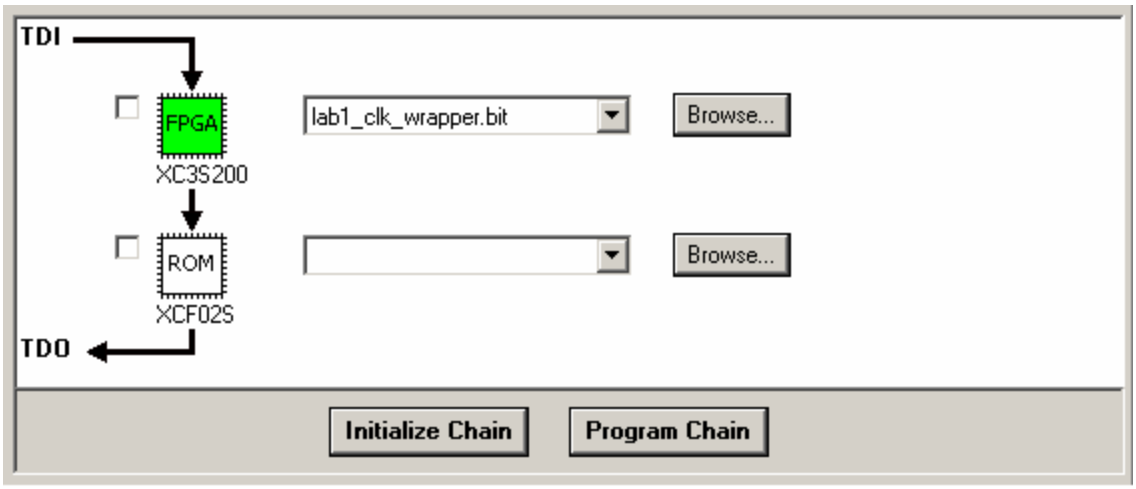
2. To power up the board connect the USB cable to the PC and flip on the switch next to the power supply port so that a red LED is lit.

3. Once the program is open, click on the **Initialize Chain** button.

4. Two chips will appear in the window. Click on the **FPGA**, since you are only programming the FPGA. It will turn green.

5. Now, go to **Browse** and in your **DSPwFPGAs** folder find and open the file **lab1inc.bit** to add it to the drop down menu. A **warning** window may appear warning that the clock for the file is 'CCLK' instead of 'JTAG CLK', select **yes**.

6. Select the **lab1inc.bit** file from the drop down menu. Click the **Program Chain** button.



G. Observing the Board

1. The switches form an eight bit input, which corresponds to the value M calculated for the prelab. Observe how changing the value of the input affects the speed of the seven segment display.

2. Turn on the oscilloscope. One channel will display the sine wave through the digital to analog converter. The second channel will display the output of the accumulator sliced to it's eight most significant bits and put through the digital to analog converter.

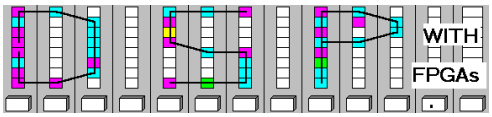
3. Determine the period length and frequency ($F=M/2^{14}*F_{in}$) of the sine wave for:

   M=1 T = _____ F=_____

   M=16 T=_____ F=_____

   M=64 T=_____ F=_____

4. Show your working FPGA board design to the lab instructor.



H. Deliverables

1) Solve the problems of the pre-lab. (3 points).

2) Print the completed schematic for the MDF file **lab1inc.mdl** and the Simulink simulation scope plot (7 points).

Make sure your name and SS is on all pages you turn in!