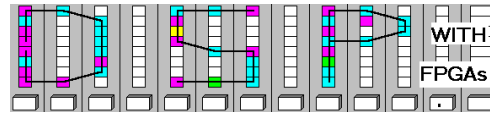


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LAB 5: Introduction to Finite Impulse Response Filters (10 points)

In this lab, you will be introduced to finite impulse response (FIR) filter design. Filters are one of the most important elements in DSP and are typically used to isolate a specific frequency band of a signal. FIR filters have low quantization sensitivity, simple structures, and can easily be made to have a linear phase response.

In the **pre-lab**, you will use “pencil-and-paper” to compute the results you expect later in your design implementation. In the **design part**, you will design a halfband filter using direct coefficient coding and reduced adder graph design. Please bring your own pair of headphones to the lab so you can hear the effects of noise and filtration.

Lab Objectives

After completing this lab you should be able to

- Design and simulate an moving average filter (MAF)
- Understand the difference between the direct-form and transposed-form of an FIR filter
- Design and simulate a reduced adder graph FIR filter using Simulink

Pre-lab (3 points)

For a moving average filter with K-taps, what should the output scaling be so that the overall gain of the filter is 1?

Gain for K-tap MAF = _____

What output scaling factor is required for a 4-tap MAF?

Gain for 4-tap MAF = _____

1. For a 3-tap MAF, determine the output values $y[n] = (x[n] + x[n-1] + x[n-2])/3$ for the input values given below. Assume zero values ($x[n], y[n]=0$) for $n < 0$ and $8 < n$.

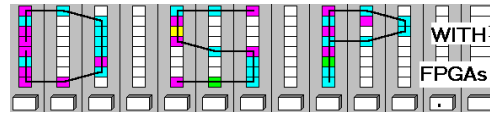
n	0	1	2	3	4	5	6	7	8
x[n]	0	4	4	2	-1	-5	-3	-4	1
y[n]									

Do you think the original signal ($x[n]$ without noise) was a sine, cosine, triangle, or square wave?

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2. Draw the impulse response using “step functions” for the following halfband filter.
(Coefficient values: $f[0] = f[10] = 9$, $f[2] = f[8] = -44$, $f[4] = f[6] = 208$, $f[5] = 348$)

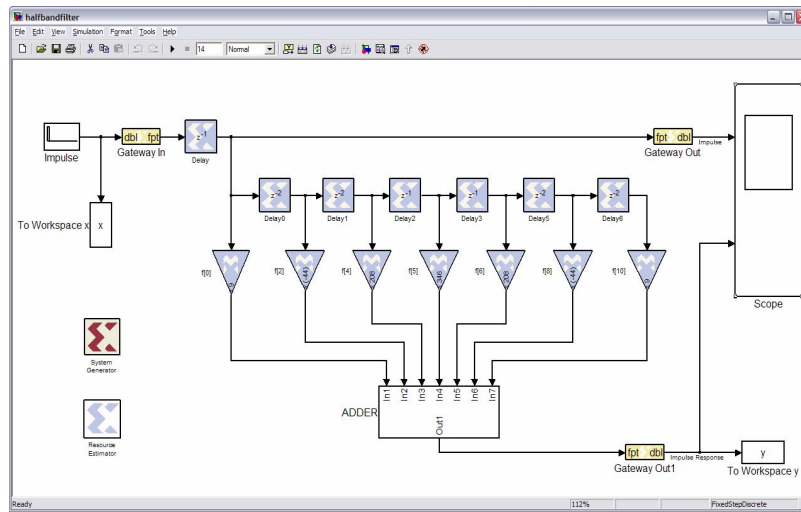


Figure 1: Halfband Filter

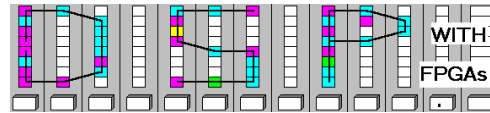


3. Determine the reduced adder graph (RAG) for a length-11 halfband filter with the following coefficients: $f[0] = f[10] = 3$, $f[2] = f[8] = -25$, $f[4] = f[6] = 150$, and $f[5] = 256$. (Hint: $150 = 2 \cdot (3 \cdot (3 \cdot 8 + 1))$)

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Simulink Design-lab



Follow the directions below to implement a moving average filter and a halfband filter.

A. Getting Started

If you are in B114 or the digital logic lab:

1. On the desktop double click on **Engineering folder**.
2. Double click on **MatLab** icon  to start **MatLab**.
3. From the top toolbar in the **MatLab** window, click on the **Simulink** icon  to start **Simulink**.
4. You should not save anything on the local hard disk. You will have to use a Zip, floppy disk, USB flash drive, or your "mapped" home directory to save the files. Create a new folder named **DSPwFPGAs** on your mapped network drive.

B. Compiling an Existing Moving Average Filter Design

1. Download the file "**maf.mdl**" from the class webpage and put the file in your **DSPwFPGAs** folder.
2. On the **MatLab** toolbar, click on the "browse for folder" icon  and select your **DSPwFPGAs** folder as the new directory.
3. The files in the **DSPwFPGAs** can now be easily accessed with the "open file" button  on the **MatLab** toolbar. Double click on the "**maf.mdl**" file and after a moment you should see the design:

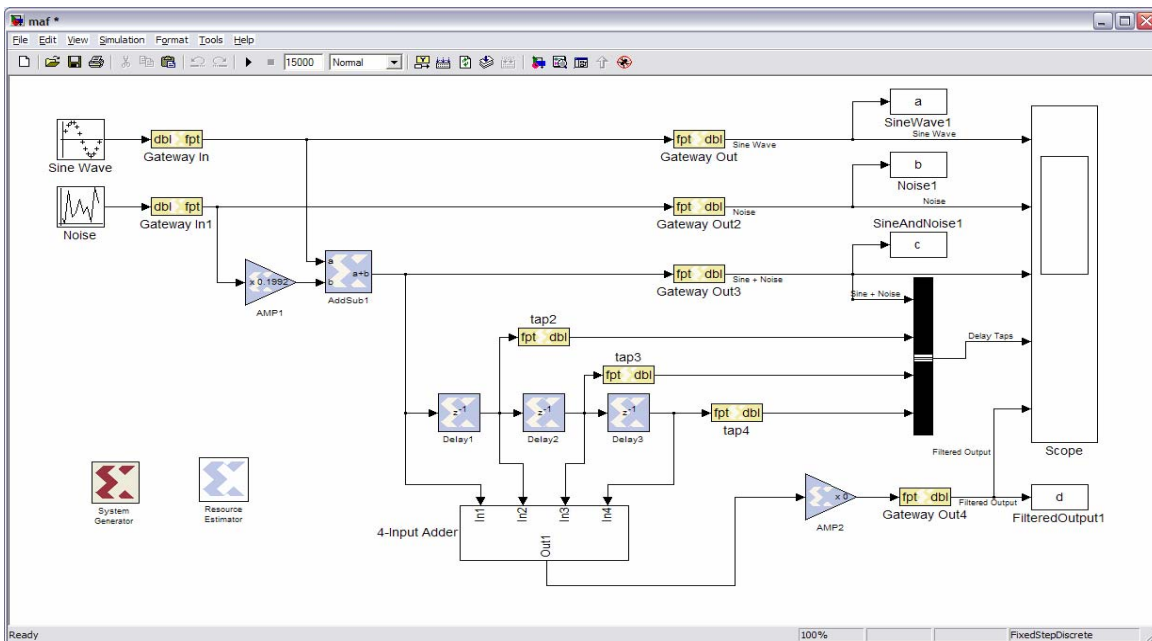
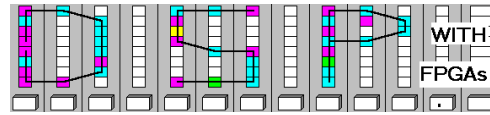



Figure 4: 4-tap moving average filter

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- Modify the gain of "AMP2" so that the overall gain of the system is 1. Carefully choose the number of fractional bits in the gain block by double-clicking on the gain block, checking "Show Constant Data Type Parameters," and entering your value in "Binary Point of Constant." Verify the correct function by simulating your design and viewing the scope output.
- The amplitude of the random noise generator amplitude is initially set to 0.2 (by "AMP1"). Press the "start simulation" button  and look at the scope output. To hear the effects of noise and filtration, plug headphones into the headphone jack (at the back of the computer) and type the following at the **MatLab** prompt:

```
> wavplay([ a.' c.' d.' c.' d.' a.' ])
```

Now, set "AMP1" to 0.9 and repeat. Can you hear the difference in the noise level?
(Note: At the **MatLab** prompt, simply press the "up" button to retype the last command.)

- What is the maximum noise amplitude this MAF can tolerate such that the output is clearly a sine function? Use the scope and your ears. (**Print** and turn in the scope output for both an acceptable noise level and an unacceptable noise level.)

Maximum Noise Amplitude = _____

C. Simulating the F5 Direct-Form Filter

- Download "F5direct.mdl" and "showfft.m" from the class webpage and put these files in your **DSPwFPGAs** folder. Open the "F5direct.mdl," and you should see the following design:

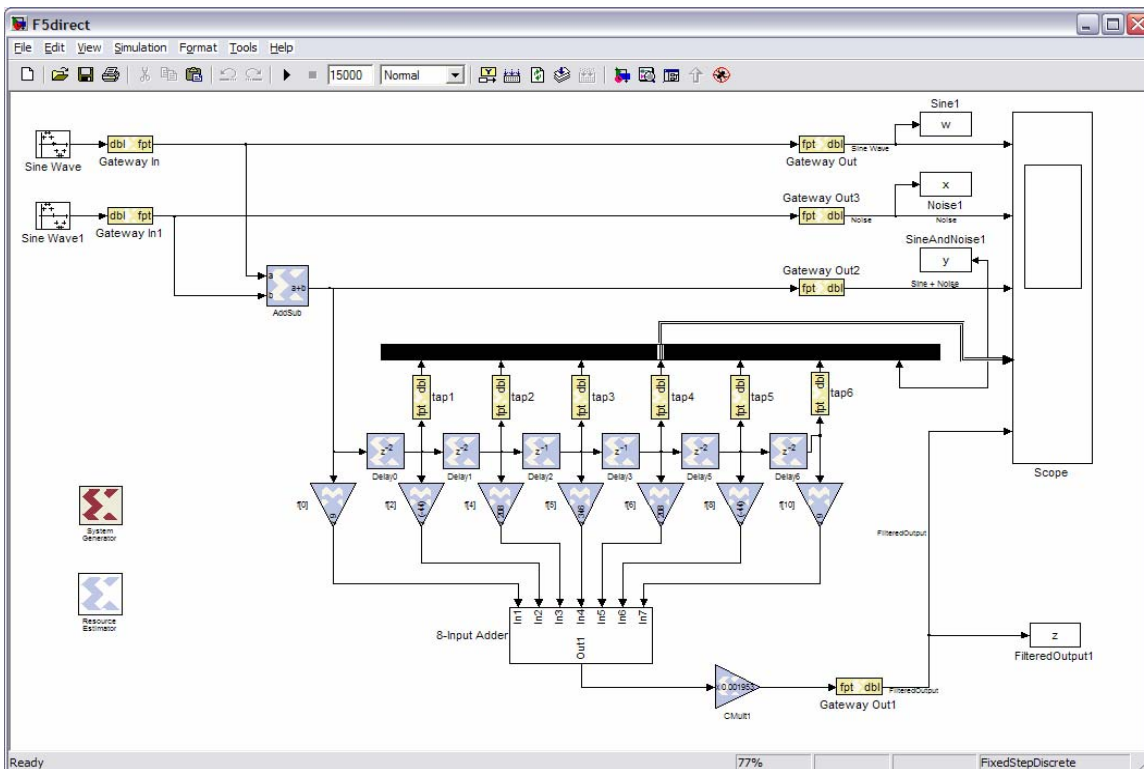
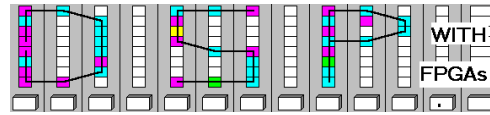


Figure 5: F5 Direct Filter

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2. Simulate "F5direct.mdl." (**Print** and turn in scope output.)
3. At the **MatLab** prompt, use the showfft(y) and showfft(z) function provided to "measure" the amplitude of the "noise" sine component before and after filtering.

Noise Magnitude Before Filtration = _____

Noise Magnitude After Filtration = _____

To hear the effects of filtration, type the following at the **MatLab** prompt:

```
> wavplay([ w.' y.' z.' y.' z.' w.' ])
```



4. To Compile the design, double-click on the **System Generator** block and ensure that the path ".\fir" exists in the "Target Directory" field. Also make sure that under "Part," you have selected the Spartan3 xc3s200-5ft256. To compile, click on **generate**. Find the new folder called "fir" that has been created in your **DSPwFPGAs** folder. Now, double-click "f5direct_clk_wrapper.ise" to open in ISE.

Right click on **Generate Programming File** near the bottom of the **processes** window to compile. Next, determine the number of required 4-input lookup tables (LUTs) by clicking on **View Design Summary**. Also, find the maximum frequency by looking at the **Post Place and Route Static Timing Report**, under **Detailed Reports** (at the bottom of the design summary). The number of required **18x18 Multipliers** and **Black RAM** can be found in the **MAP Report**.

Total 4 input LUTs = _____

Block RAMs = _____

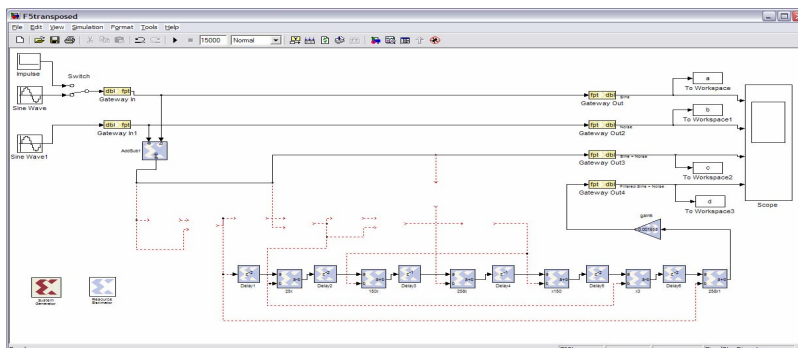
Multipliers 18x18s = _____

Max. Freq. = _____

D. Complete the R5 RAG Simulink Design

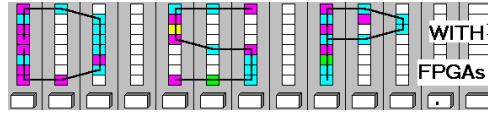
The direct-form FIR filter can be optimized in several ways. First, we can use a constant coefficient multiplier block (called gain) instead of the general-purpose multiplier. Or, we could use the transposed FIR form to reduce the adder delay. Another way would be to combine the coefficients using the reduced adder graph (RAG) you developed in the pre-lab.

1. Download "F5transposed.mdl" from the class webpage and put the file in the **DSPwFPGAs** folder.
2. Complete the design (i.e. add your reduced adder graph) and simulate. **Print** your design and simulation.



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Figure 5: Incomplete F5 transposed SFG.

3. Simulate the design in **Simulink** to verify the functionality. (**Print** scope output to turn in.)
4. Follow the instructions in part C-4 to compile the design using **System Generator** and determine:

Total 4 input LUTs = _____

Block RAMs = _____

Multipliers 18x18s = _____

Max. Freq. = _____

5. Compare this design with the direct form design f5direct.mdl. Determine the improvements:

4-Input LUTs Improvement = _____%

Max. Freq. Improvement = _____%

F. Deliverables:

1. Solve the problems of the pre-lab. (3 points).
2. Print the MDL files and the Simulink simulations from parts B-6, C-2, and D-2. (7 points).

Make sure your name and SS is on all pages you turn in!