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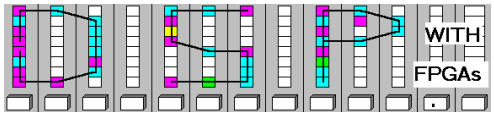
LABORATORY
Introduction to SFGs



LAB 3: Introduction to Signal Flow Graphs
(10 Points)

In this lab, you will be introduced to Signal Flow Graphs (SFGs), system analysis, and system synthesis. DSP systems can be described by different methods. Most frequently used are the differential equation, the z-transform, and the SFG. When designing a system, it is very important to analyze the system's properties mathematically, which can be done by the three methods noted above.

In the **pre-lab**, you will use "pencil and paper" to compute the results you expect later in your design implementation. In the **design part**, you will design three systems and analyze their responses to an impulse sequence.

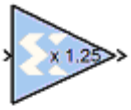
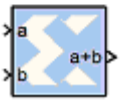
Lab Objectives

After completing this lab, you should be able to:

- Characterize systems by their linearity, stability, causality, and time-invariance.
- Understand the difference between FIR and IIR systems.
- Design and simulate FIR and IIR systems using Simulink with the Xilinx blockset.

Pre-Lab (5 Points)

1. SFGs are built using basic building blocks. Give a short description and the corresponding difference equation for the 5 blocks below. The gain block is given as an example. Use a[n] and b[n] as the inputs and *y*[n] as the output.

Element	Description	Difference Equation
 Block 1	Scaling with a constant value of 1.25	y[n] = 1.25•a[n]
 Block 2		y[n] =
 Block 3		y[n] =
 Block 4		y[n] =
 Block 5		y[n] =

2. For each of the three systems shown below, determine the response to the two-impulse sequence shown in figure 2 (amplitudes are +10 and -20). Also note that the "1,0,1,0... Sequence" block of System 1 produces a repeating length-two sequence of 1's and 0's.

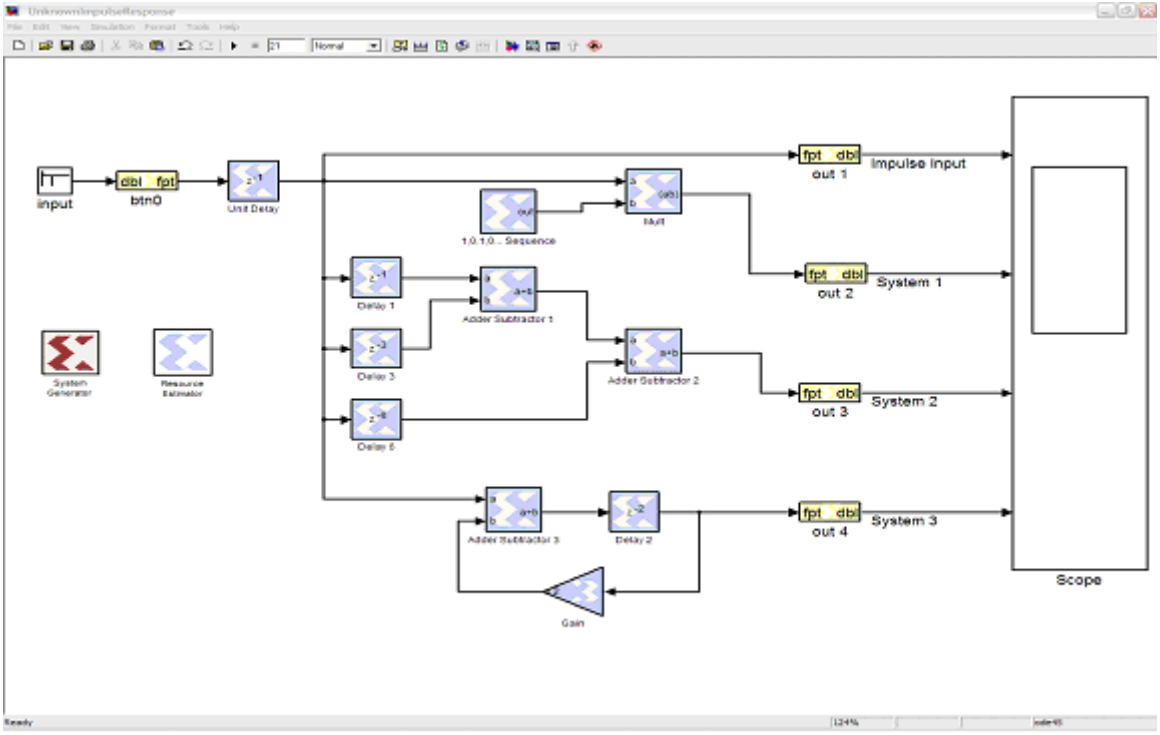


Figure 1: Three systems with unknown impulse responses

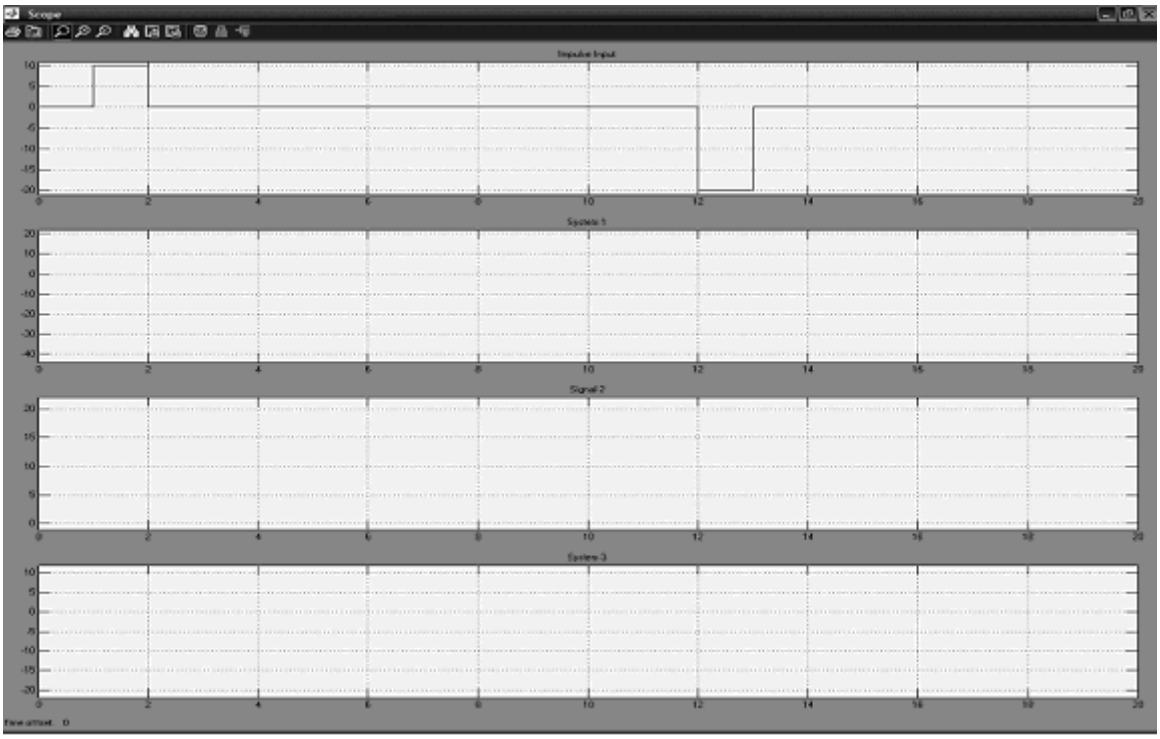


Figure 2: Scope plot for the three impulse responses

3. The following figure shows three black box systems. The SFG of the each system is unknown, but their responses to an impulse sequence of +10 and -20 have been measured and are shown in Figure 4. Use the given impulse responses to determine the difference equations of the systems, and then fill in the missing SFGs in Figure 3.

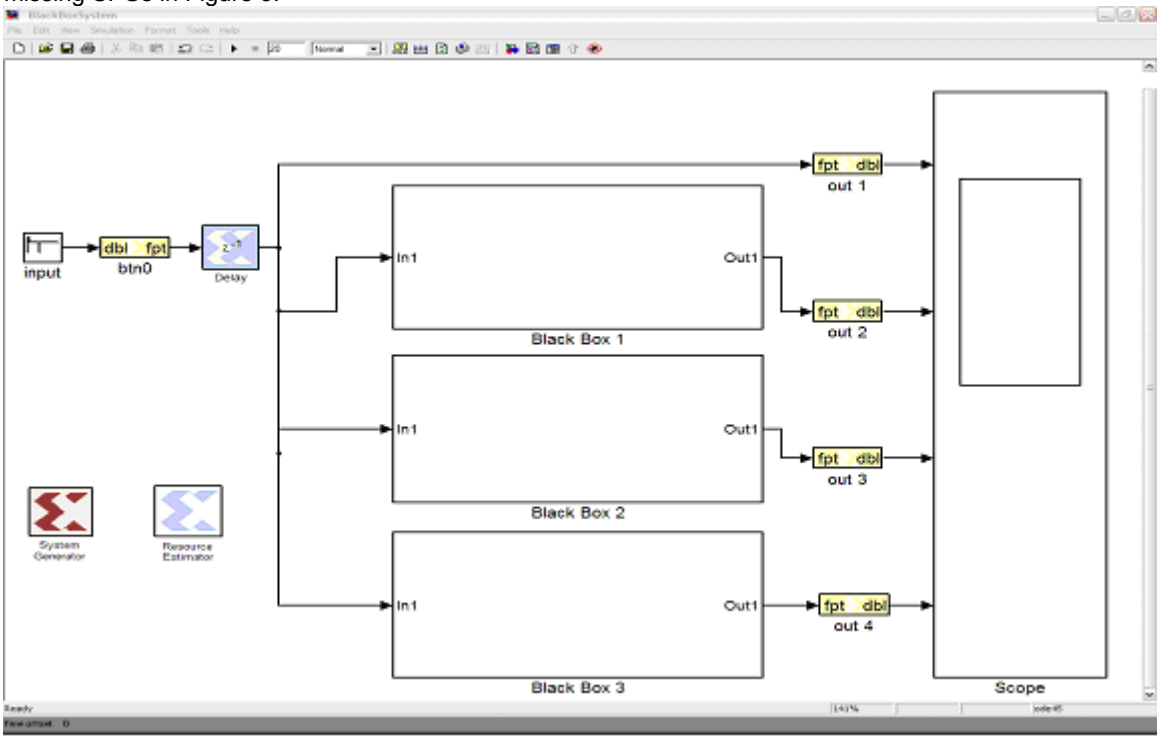
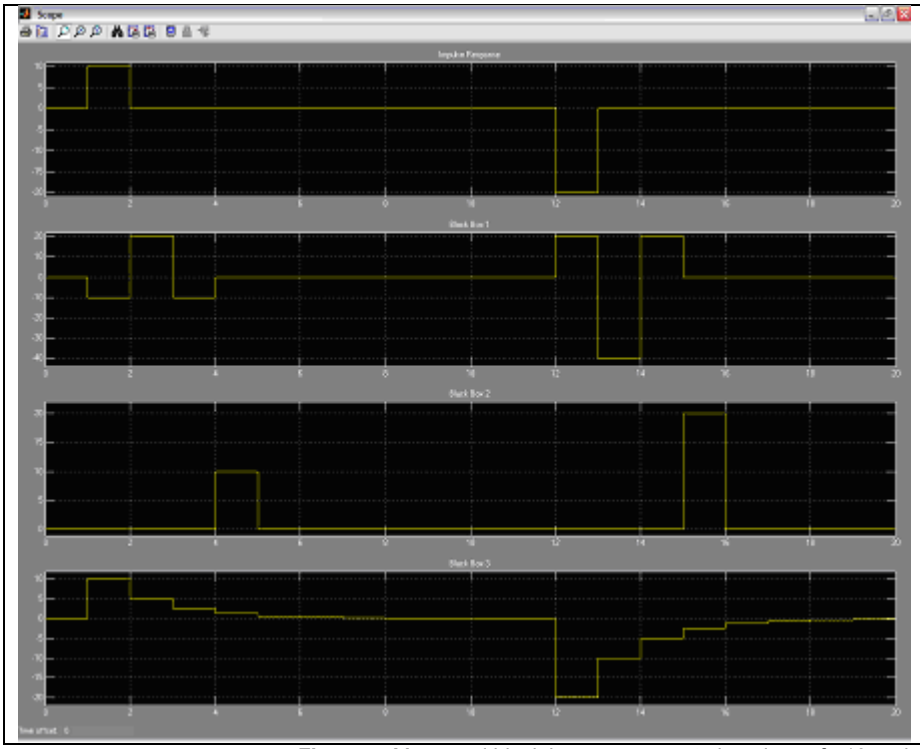


Figure 3: Black box systems with known impulse responses



Black Box 1: y[n]=
Black Box 2: y[n] =
Black Box 3: y[n] =

Figure 4: Measured black box responses to impulses of +10 and -20

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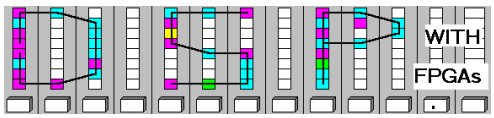
LABORATORY
Introduction to SFGs



Simulink Design-lab (5 points)

Follow the directions below to implement the circuit shown in Fig. 3.

A. Getting Started

If you are in B114 or the Digital Logic Lab:

1. On the desktop double click on **Engineering folder**.
2. Double-click on the **MatLab** icon  to start **MatLab.**
3. From the top toolbar in the **MatLab** window, click on the **Simulink** icon  to start **Simulink.**
4. You should not save anything on the local hard disk. You will have to use your own Zip, floppy disk, USB flash drive, or your "mapped" home directory to save the files. Create a New Folder named **DSPwFPGAs** on your mapped network drive.

B. Design the SFG systems

1. Download the file "sfg.mdl" from the class webpage and put the file in your **DSPwFPGAs** folder.
2. On the **MatLab** toolbar, click on the "browse for folder" icon  and select your **DSPwFPGAs** folder as the new directory.
3. The files in the **DSPwFPGAs** can now be easily accessed with the "open file" button  on the **MatLab** toolbar**.** Double click on the "**sfg.mdl**" file and after a moment you should see the design:

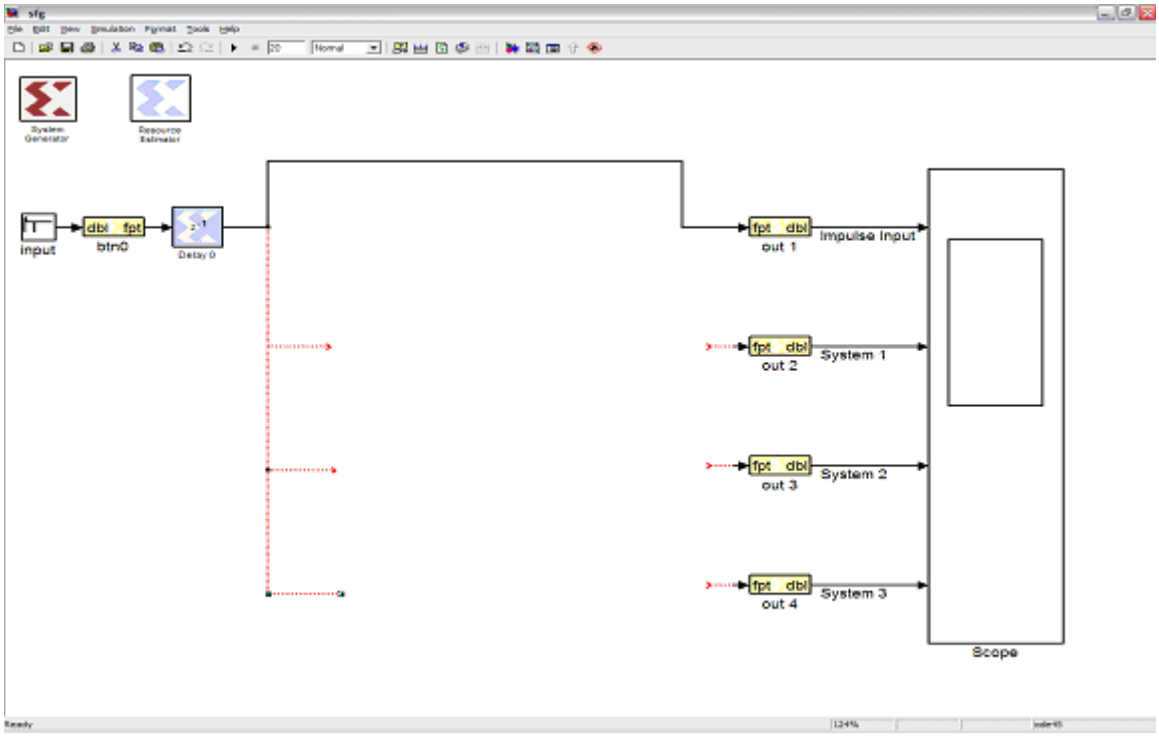
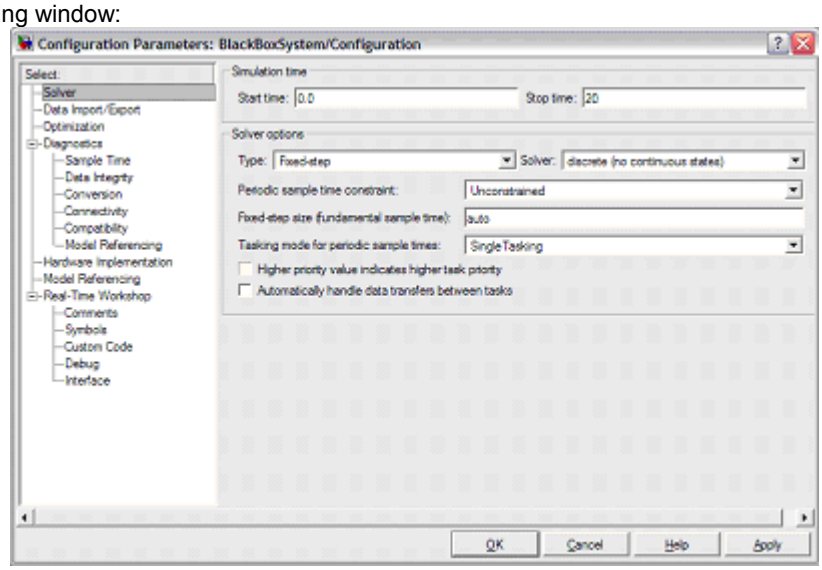


Figure 5: Incomplete design.

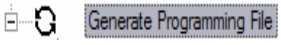
C. Completion of the SFG Design

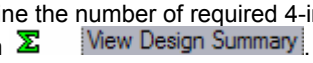
1. Add the design you developed in the pre-lab for the black-box system. Use elements from the Xilinx Blockset (found in the **Simulink** library browser ).

2. Verify your design via a **Simulink** simulation. Make sure the impulse responses match those from part 3 of the pre-lab! Set the correct simulation parameters by clicking "Simulation" on the **Simulink** toolbar and then "Configuration Parameters." Match the solver settings to those in the following window:



3. To Compile the design, double-click on the **System Generator** block  and ensure that the path "**./sfg**" exists in the "Target Directory" field. Also make sure that under "Part," you have selected the Spartan3 xc3s200-5ft256. To compile, click on **generate**. Find the new folder called "**sfg**" that has been created in your **DSPwFPGAs** folder. Now, double-click "**sfg_clk_wrapper.ise"** to open in ISE.

   Right click on 

near the bottom of the **processes** window to compile. Next, determine the number of required 4-input lookup tables (LUTs), BlockRAMs and Multipliers by clicking on 

. Also, find the maximum frequency by looking at the **Post Place and Route Static Timing Report,** under **Detailed Reports** (at the bottom of the design summary).

   4 input LUTs = _____

   Block RAMs =_____

   Multipliers 18x18s =_____

   Max. Freq. = _____

D. Deliverables

1. Solve the problems from the pre-lab (5 points)

2. Print your completed sfg.mdl file and the correct **Simulink** scope output (5 points).

Make sure your name and SS number is on all pages!